HD46508, HD46508-1, HD46508A, HD46508A-1

ADU (Analog Data Acquisition Unit)

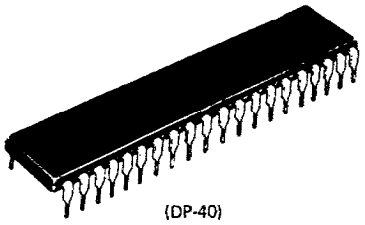
The HD46508 is a monolithic NMOS device with a 10-bit analog-to-digital converter, a programmable voltage comparator, a 16-channel analog multiplexer and HMCS6800 microprocessor family compatible interface.

Each of 16 analog inputs is either converted to a digital data by the analog-to-digital converter or compared with the specified value by the programmable comparator. The analog-to-digital converter uses successive approximation method as the conversion technique. It's intrinsic resolution is 10 bits but it can be 8 bits if the programmer so desires. The programmable voltage comparator compares the input voltage with the value specified by the programmer. The result (greater than, or smaller than) is reflected to the flag in the status register.

The device can expand its capability by controlling the external circuits such as sample holder, pre-amplifier and external multiplexer.

With these features, this device is ideally suited to applications such as process control, machine control and vehicle control.

HD46508P, HD46508P-1, HD46508PA, HD46508PA-1

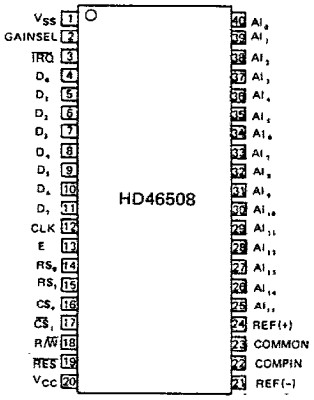


(DP-40)

■ FEATURES

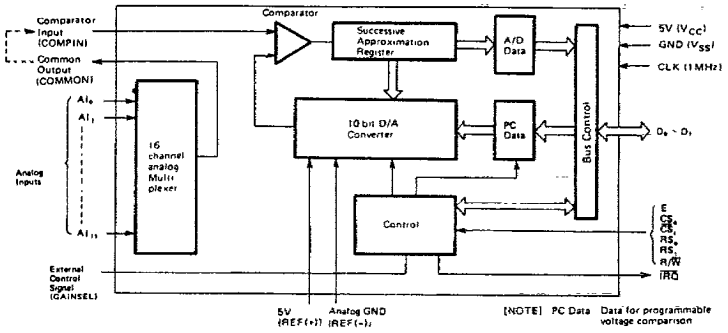
- 16-channel Analog multiplexer
- Programmable A/D Converter resolution (10-bit or 8-bit)
- Programmable Voltage comparison (PC)
- Conversion Time 100μs (A/D), 13μs(PC)
- External Sample and Hold Circuit Control
- Auto Range-switching Control of External Amplifier
- Waiting Function for the Settling Time of External Amplifier
- Interrupt Control (Only for A/D conversion)
- Single +5V Power Supply
- Compatible with HMCS6800 Bus (The connection with other Asynchronous Buses possible)

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ORDERING INFORMATION

ADU	Bus Timing	Non Linearity*
HD46508A	1 MHz	±1 LSB
HD46508A-1	1.5 MHz	
HD46508	1 MHz	±3 LSB
HD46508-1	1.5 MHz	

* Specification for 10 bit A/D conversion

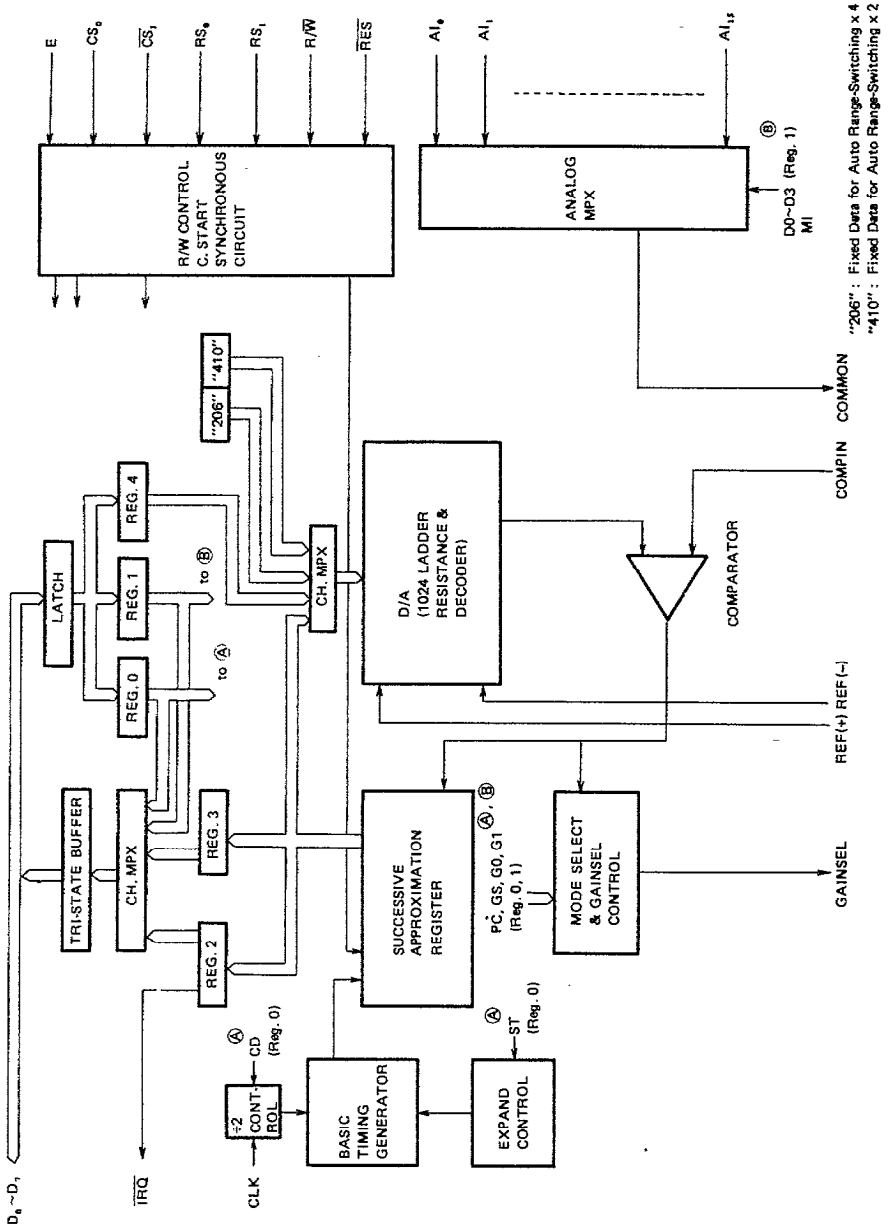


Figure 1 Internal Block Diagram

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{CC}*	−0.3 ~ +7.0	V
Input Voltage	V_{in}*	−0.3 ~ +7.0	V
Analog Input Voltage	V_{AIn}*	−0.3 ~ +7.0	V
Operating Temperature	T_{opr}	− 20 ~ + 75	°C
Storage Temperature	T_{stg}	− 55 ~ +150	°C

* With respect to V_{SS} (SYSTEM GND)

[NOTE] Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}*	4.75	5.0	5.25	V
Input "High" Voltage	V_{IH}*	2.0	–	V_{CC}	V
Input "Low" Voltage	V_{IL}*	−0.3	–	0.8	V
Analog Input Voltage	V_{Ain}*	0	–	$V_{REF(+)}$	V
Reference Voltage	$V_{REF(+)}$*	–	V_{CC}	V_{CC}+0.25	V
	$V_{REF(-)}$*	−0.1	0	–	
Voltage Center of Ladder	$\frac{V_{REF(+)} + V_{REF(-)}}{2}$*	–	$\frac{V_{CC}}{2}$	$\frac{V_{CC}}{2}$+0.25	V
Operating Temperature	T_{opr}	− 20	25	75	°C

*With respect to V_{SS} (SYSTEM GND)

■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS <1> (V_{CC} = 5V ± 5%, V_{SS} = 0V, Ta = −20 ~ +75°C, unless otherwise noted.)

Item		Symbol	Test Condition	min	typ	max	Unit
Input "High" Voltage		V_{IH}		2.0	–	V_{CC}	V
Input "Low" Voltage		V_{IL}		−0.3	–	0.8	V
Output "High" Voltage	D_0 ~ D_7	V_{OH}	I_{OH} = −205μA	2.4	–	–	V
	GAINSEL		I_{OH} = −200μA	2.4	–	–	
			I_{OH} = −10μA	V_{CC}−1.0	–	–	
Output "Low" Voltage	D_0~D_7, GAINSEL	V_{OL}	I_{OL} = 1.6 mA	–	–	0.4	V
	$\overline{IRQ}$		I_{OL} = 3.2 mA	–	–	0.4	
Input Leakage Current	E, CLK, R/$\overline{W}$ $\overline{RES}$, RS_0, RS_1 CS_0, $\overline{CS_1}$	I_{in}	V_{in} = 0 ~ 5.25V	−2.5	–	2.5	μA
Three-State (off state) Input Current	D_0 ~ D_7	I_{TSI}	V_{in} = 0.4 ~ 2.4V	−10	–	10	μA
Output Leakage Current	$\overline{IRQ}$	I_{LOH}	V_{OH} = 2.4V	–	–	10	μA
Power Dissipation		P_D		–	–	500	mW
Input Capacitance	D_0 ~ D_7	C_{in}	V_{in} = 0V, Ta = 25°C f = 1 MHz	–	–	12.5	pF
	E, CLK, R/$\overline{W}$ $\overline{RES}$, RS_0, RS_1 CS_0, $\overline{CS_1}$			–	–	10.0	pF
Output Capacitance	$\overline{IRQ}$, GAINSEL	C_{out}	V_{in} = 0V, Ta = 25°C f = 1 MHz	–	–	10.0	pF

- **DC CHARACTERISTICS <2> (V_{CC} = 5V ± 5%, V_{SS} = 0V, Ta = −20~+75°C, unless otherwise noted.)**

Item	Test Condition	min	typ	max	Unit
Analog Multiplexer ON Resistance	V_{Ain} = 5.0V, V_{CC} = 4.75V, Ta = 25°C	–	–	1	kΩ
OFF Channel Leakage Current	V_{Ain} = 5.0V V_{CC} = 4.75V, Ta = 25°C COMMON = 0V	–	10	100	nA
	V_{Ain} = 0V, Ta = 25°C V_{CC} = 4.75V, COMMON = 5V	−100	−10	–	nA
Analog Multiplexer Input Capacitance		–	–	7.5	pF
Ladder Resistance (from REF(+) to REF(−))	$V_{REF\ (+)}$ = 5.0V $V_{REF\ (-)}$ = 0V, Ta = 25°C	10	–	40	kΩ

- **CONVERTER SECTION (Ta = 25°C, V_{CC} = $V_{REF(+)}$ = 5.0V, t_{cycC} = 1μs, unless otherwise noted.)**

1. 10-BIT A/D CONVERSION

Item	HD46508A, HD46508A-1			HD46508, HD46508-1			Unit
	min	typ	max	min	typ	max	
Resolution	–	10	–	–	10	–	bits
Non-linearity Error *	–	±1/2	±1	–	±1	±3	LSB
Zero-Error	–	±1/2	±3/4	–	±1/2	±1	LSB
Full-Scall Error	–	±1/4	±1/2	–	±1/2	±1	LSB
Quantization Error	–	–	±1/2	–	–	±1/2	LSB
Absolute Accuracy *	–	±1	±3/2	–	±2	±4	LSB

2. 8-BIT A/D CONVERSION

Item	HD46508A, HD46508A-1			HD46508, HD46508-1			Unit
	min	typ	max	min	typ	max	
Resolution	–	8	–	–	8	–	bits
Non-linearity Error *	–	±1/8	±1/4	–	±1/4	±3/4	LSB
Zero-Error	–	±1/4	±3/8	–	±3/8	±1/2	LSB
Full-Scall Error	–	±1/4	±3/8	–	±3/8	±1/2	LSB
Quantization Error	–	–	±1/2	–	–	±1/2	LSB
Absolute Accuracy *	–	±5/8	±3/4	–	±3/4	±5/4	LSB

3. PROGRAMMABLE VOLTAGE COMPARISON (PC)

Item	HD46508A, HD46508A-1			HD46508, HD46508-1			Unit
	min	typ	max	min	typ	max	
Resolution	–	8	–	–	8	–	bits
Non-linearity Error *	–	±1/8	±1/4	–	±1/4	±3/4	LSB
Zero-Error	–	±1/4	±3/8	–	±3/8	±1/2	LSB
Full-Scall Error	–	±1/4	±3/8	–	±3/8	±1/2	LSB
Absolute Accuracy *	–	±3/8	±5/8	–	±1/2	±1	LSB

*Temperature Coefficient: 25 ppm of FSR/°C (max)

● **AC CHARACTERISTICS (V_{CC} = 5.0V ± 5%, V_{SS} = 0V, Ta = −20 ~ +75°C, unless otherwise noted.)**

1. CLOCK WAVEFORM

Item	Symbol	Test Conditions	CD* = 0			CD* = 1			Unit
			min	typ	max	min	typ	max	
CLK Cycle Time	t_{cycC}	Fig. 2	1.0	–	10	0.5	–	5	μs
CLK "High" Pulse Width	PW_{CH}		0.45	–	4.5	0.22	–	2.2	μs
CLK "Low" Pulse Width	PW_{CL}		0.40	–	4.0	0.21	–	2.1	μs
Rise and Fall Time of CLK	t_{Cr}, t_{Cf}		–	–	25	–	–	25	ns

* CD : CLK Divider bit

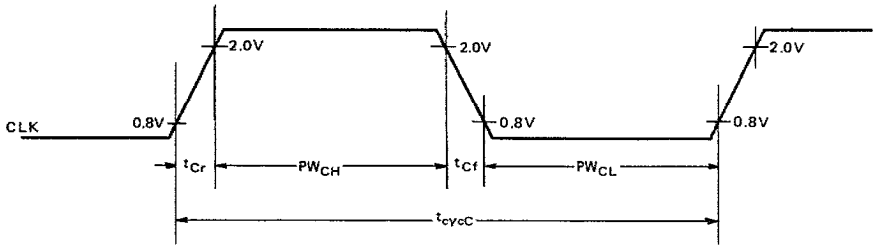


Figure 2 CLK Waveform

2. $\overline{IRQ}$, GAINSEL OUTPUT

Item	Symbol	Test condition	min	typ	max	Unit
$\overline{IRQ}$ Release Time	t_{IR}	Fig. 3	–	–	750	ns
GAINSEL Delay Time	t_{GSD1}	Fig. 4	–	–	750	ns
	t_{GSD2}		–	–	750	ns

t_{GSD1} : TTL Load
t_{GSD2} : CMOS Load

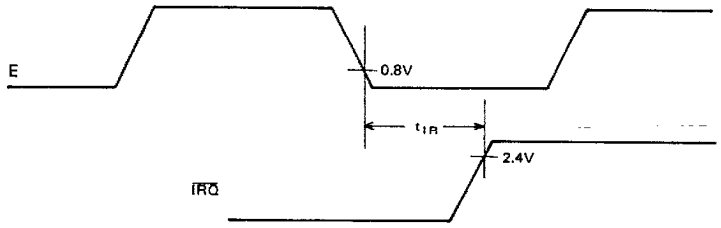
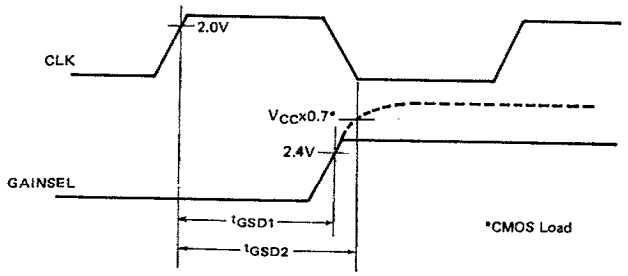


Figure 3 $\overline{IRQ}$ Release Time

(1) Sample & Hold



(2) x2, x4 Auto Range-Switching, Programmable Gain

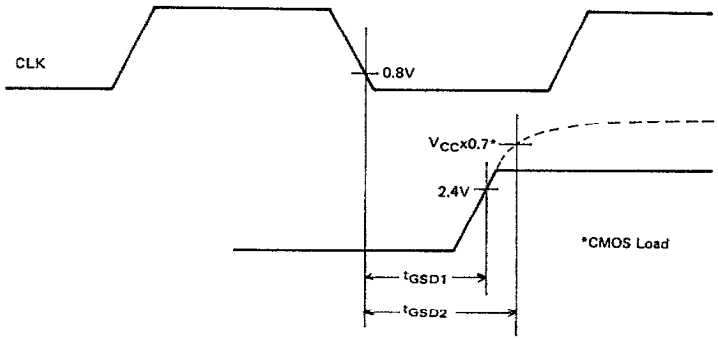


Figure 4 GAINSEL Delay Time

3. BUS TIMING CHARACTERISTICS

READ OPERATION SEQUENCE

Item	Symbol	Test Condition	HD46508 HD46508A			HD46508-1 HD46508A-1			Unit
			min	typ	max	min	typ	max	
Enable Cycle Time	t_{cycE}	Fig. 5	1.0	–	–	0.666	–	–	μs
Enable "High" Pulse Width	PW_{EH}		0.45	–	–	0.28	–	–	μs
Enable "Low" Pulse Width	PW_{EL}		0.40	–	–	0.28	–	–	μs
Rise and Fall Time of Enable	t_{Er},t_{Ef}		–	–	25	–	–	25	ns
Address Set Up Time	t_{AS}		140	–	–	140	–	–	ns
Data Delay Time	t_{DDR}		–	–	320	–	–	220	ns
Data Access Time	t_{ACC}		–	–	460	–	–	360	ns
Data Hold Time	t_H		10	–	–	10	–	–	ns
Address Hold Time	t_{AH}		10	–	–	10	–	–	ns

WRITE OPERATION SEQUENCE

Item	Symbol	Test Condition	HD46508 HD46508A			HD46508-1 HD46508A-1			Unit
			min	typ	max	min	typ	max	
Enable Cycle Time	t_{cycE}	Fig. 6	1.0	–	–	0.666	–	–	μs
Enable "High" Pulse Width	PW_{EH}		0.45	–	–	0.280	–	–	μs
Enable "Low" Pulse Width	PW_{EL}		0.40	–	–	0.280	–	–	μs
Rise and Fall Time of Enable	t_{Er}, t_{Ef}		–	–	25	–	–	25	ns
Address Set Up Time	t_{AS}		140	–	–	140	–	–	ns
Data Set Up Time	t_{DSW}		195	–	–	80	–	–	ns
Data Hold Time	t_H		10	–	–	10	–	–	ns
Address Hold Time	t_{AH}		10	–	–	10	–	–	ns

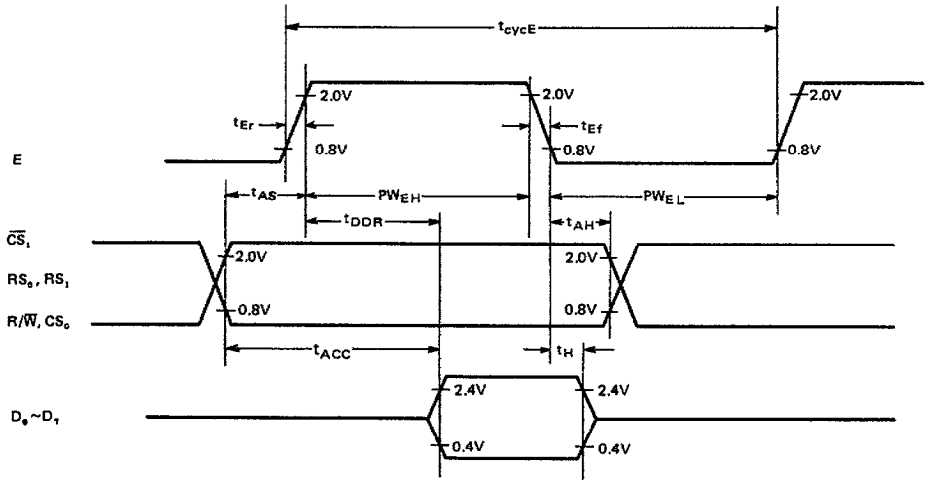


Figure 5 Read Timing

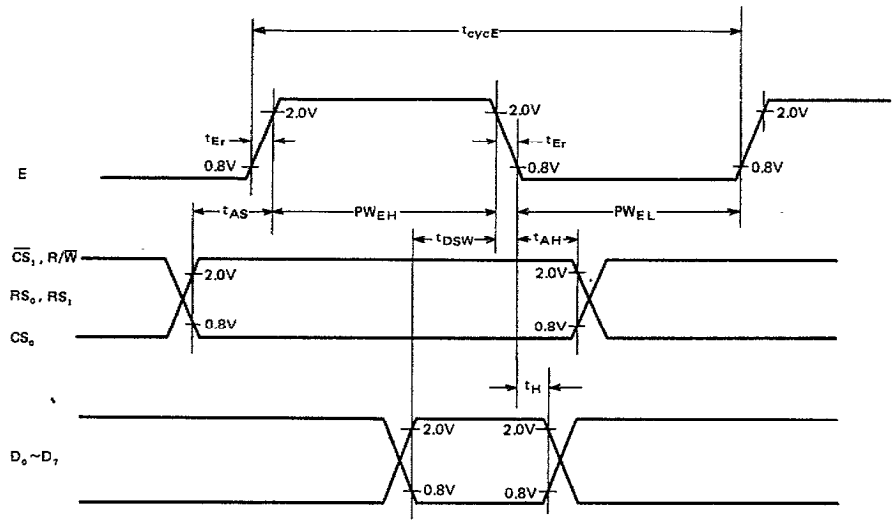


Figure 6 Write Timing

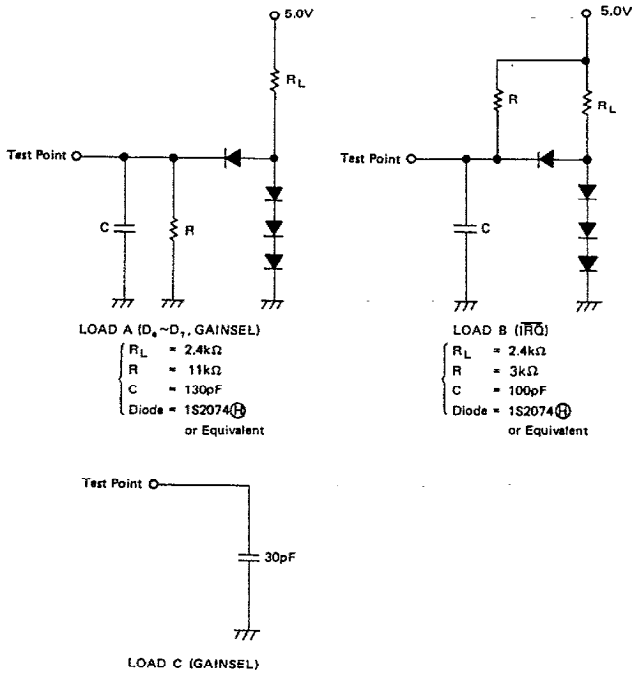


Figure 7 Test Load

■ SIGNAL DESCRIPTION

• Processor Interface

Data Bus (D_0~D_7)

The Bi-directional data lines (D_0~D_7) allow data transfer between the ADU and MPU. Data bus output drivers are three state buffers that remain in the high-impedance state except when MPU performs a ADU read operation.

Enable (E)

The Enable signal (E) is used as strobe signal in MPU R/W operation with the ADU internal registers. This signal is normally derived from the HMCS6800 system clock (ϕ_2).

Chip Select (CS_0, $\overline{CS_1}$)

The Chip Select lines (CS_0, $\overline{CS_1}$) are used to address the ADU. The ADU is selected when CS_0 is at "High" and $\overline{CS_1}$ is at "Low" level.

Read/Write (R/$\overline{W}$)

The R/$\overline{W}$ line controls the direction of data transfer between the ADU and MPU. When R/$\overline{W}$ is at "High" level, data of ADU is transferred to MPU. When R/$\overline{W}$ is at "Low" level, data of MPU is transferred to ADU.

Register Select (RS_0, RS_1)

The Register Select line (RS_0, RS_1) are used to select one of the 4 ADU internal registers. Table 1 shows the relation between (RS_0, RS_1) address and the selected register. The lowest 2 address lines of MPU are usually used for these signals.

Reset ($\overline{RES}$)

This input is used to reset the ADU. An input "Low" level on $\overline{RES}$ line forces the ADU into following status.

1) All the shift-registers in ADU are cleared and the conversion operation is stopped.
2) The GAINSEL output goes down to "Low" level. The $\overline{IRQ}$ output is made "Off" state and the D_0~D_7 are made high impedance state.

Interrupt Request ($\overline{IRQ}$) (Open Drain Output)

This output line is used to inform the A/D conversion end signal to the MPU. This signal becomes active "Low" level when IE bit in the control register 1 is "1" and IRQ bit in the control register 2 goes "1" at the end of conversion. And this signal returns to "High" right after The MPU reads the A/D Data Register (R3). Programmable voltage comparison does not affect this signal.

• Analog Data Interface

Analog Input (AI_0~AI_{15})

The Input Analog Data to be measured is applied to these Analog Input (AI_0~AI_{15}). These are multiplexed by internal 16 channel multiplexer and output to COMMOM pin. A particular input channel is selected when the multiplexer channel address is programmed into the control Register 1 (R1).

Multiplexer Common Output (COMMON)

This signal is the output of the 16 channel analog multiplexer, and may be connected to the input of pre-amplifier or sample/hold circuit according to user's purposes. When no external circuit needed, this output should be connected to the COMPIN input.

Comparator Input (COMPIN)

This is a high impedance input line that is used to transmit selected analog data to comparator. The COMMON line is usually connected to this input. When external Pre-amplifier or Sample/hold circuit is used, output of these circuits may be connected to this input.

Reference Voltage (+) (REF (+))

This line is used to apply the standard voltage to the internal ladder resistors.

Reference Voltage (–) (REF (–))

This line is connected to the analog ground.

• ADU Control

Conversion Clock (CLK)

The CLK is a standard clock input signals which defines internal timing for A/D conversion and PC operation.

Gain Select (GAINSEL) (CMOS Compatible Output)

This output is used to control the external circuit. The function of this signal is programmable and it is specified by (G1, G0) bits in Control Register 0. By using this output, user can control the auto-range-switching of external pre-amplifier, also control external sample & hold circuit, etc. as well.

[NOTE] This LSI is different from other HMCS6800 family LSIs in following function
- $\overline{RES}$ doesn't affect IE bit of R0

■ FUNCTION OF INTERNAL REGISTERS

• Structure

Table 1 Internal Registers of the ADU

$\overline{CS_1}$	CS_0	RS_1	RS_0	Reg. #	Register Name	Read	Write	Data Bit 7	6	5	4	3	2	1	0
0	1	0	0	R0	Control Register 0	O	O	IE	CD	ST				G1	G0
0	1	0	1	R1	Control Register 1	O	O	SC	GS	PC	MI	D3	D2	D1	D0
0	1	1	0	R2	Status & A/D Data Register (H)	O	x	IRQ	BSY	PCO		OV	DW	C9	C8
0	1	1	1	R3	A/D Data Register (L)	O	x	C7	C6	C5	C4	C3	C2	C1	C0
0	1	1	1	R4	PC Data Register	x	O	B7	B6	B5	B4	B3	B2	B1	B0

(Note) O ---YES
x ---NO

Control Register 0 (R0)

7	6	5	4	3	2	1	0
IE	CD	ST				G1	G0

	"1"	"0"
Mode Select	See Table 2	
Not Used		
Not Used		
Not Used		
Settling Time	Available	Not Available
CLK Divider	CLK/2	CLK
Interrupt Enable*	Enable IRQ	Mask IRQ

Figure 8 Control Register 0

*$\overline{RES}$ doesn't affect IE bit.

Control Register 1 (R1)

7	6	5	4	3	2	1	0
SC	GS	PC	MI	D3	D2	D1	D0

	"1"	"0"
MPX Channel Address	See Table 3	
MPX Inhibit	Inhibited	Not Inhibited
Prog. Comparator Select	Prog. Comparator mode	A/D Converter mode
GAINSEL Enable	GAINSEL Enable	GAINSEL Disable
Short-cycle Conversion	8-bit Length	10-bit Length

Figure 9 Control Register 1

Status & A/D Data Register (H)

7	6	5	4	3	2	1	0
IRQ	BSY	PCO		OV	DW	C9	C8

	"1"	"0"
Upper bit (10 bit data)		
Data Weight	See Table 4.	
Data Over Scale flag	Data is over scale	Within the scale
Not Used		
Programmable Comparator Output	$V_{Ain} > V_p$	$V_{Ain} < V_p$
Busy flag	Under Conversion	Conversion Completed
IRQ flag	Requested	Not Requested

V_{Ain} : Unknown Input Voltage
V_p : Programmed Voltage by R4

C9, C8 bits are cleared when 8 bit A/D conversion is performed.

Figure 10 Status & A/D Data Register (H)

A/D Data Register (L)

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0

Lower order 8 bit Data (Normal 10 bit Conversion)
8 bit Data (8 bit Short-cycle Conversion)

Figure 11 A/D Data Register (L)

PC Data Register

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

8 bit Data for Programmable Voltage Comparison

Figure 12 PC Data Register

- **Description for the Internal Registers**

Control Register 0 (R0)

This Register is a 5-bit read/write register that is used to specify Interrupt Enable (IE), CLK Divider (CD), Settling Time (ST) and Mode Select (G0, G1). This Register should be written before writing R1.

IE bit: (Interrupt Enable)
- IE = "1", Interrupt is requested through the $\overline{IRQ}$ output.
- IE = "0", Interrupt is masked.

CD bit: (Clock Divider)
- CD = "1", CLK ÷ 2 is used as internal clock.
- CD = "0", CLK is used directly.

ST bit: (Settling Time)
- ST = "1", First comparison is executed after 1 expanded cycle in order to compensate external amplifiers settling delay.
- ST = "0", Cycle is not delayed.

G0, G1 bit; (Mode select)
These bits are used to specify the function of GAINSEL signal when GS bit is "1".

Table 2 Function of G0, G1

G1	G0	Mode Select
0	0	Sample & Hold
0	1	Auto Range-Switching x 2
1	0	Auto Range-Switching x 4
1	1	Programmable Gain Control

Control Register 1 (R1)

This register is an 8-bit read/write register that is used to store the command for A/D conversion mode and programmable comparison mode. This register includes MPX channel address (D_0~D_3), MPX inhibit (MI), programmable comparator select (PC), GAINSEL enable (GS) and short-cycle conversion (SC) bits. When this register (R1) is programmed, each conversion mode starts.

SC bit (Short-cycle)
- SC = "1", Short-cycle conversion (8 bit length)
- SC = "0", Normal conversion (10 bit length)

GS bit (GAINSEL Enable)
- GS = "1", GAINSEL signal is enabled. The function of GAINSEL is specified by (G0, G1) bits.
- GS = "0", GAINSEL signal is disabled. ("Low" level)

PC bit (Program comparator)
- PC = "1", Programmable voltage comparator mode
- PC = "0", A/D conversion mode

MI bit (MPX Inhibit)
- MI = "1", Internal MPX channel is inhibited in order to use external MPX channel.
- MI = "0", Internal MPX channel is used.

D0~D3 (MPX channel)
These bits are used to select the particular MPX channel.

Table 3 MPX Channel Addressing

Channel #1	D3	D2	D1	D0	Analog Input
0	0	0	0	0	AI_0
1	0	0	0	1	AI_1
2	0	0	1	0	AI_2
3	0	0	1	1	AI_3
4	0	1	0	0	AI_4
5	0	1	0	1	AI_5
6	0	1	1	0	AI_6
7	0	1	1	1	AI_7
8	1	0	0	0	AI_8
9	1	0	0	1	AI_9
10	1	0	1	0	AI_{10}
11	1	0	1	1	AI_{11}
12	1	1	0	0	AI_{12}
13	1	1	0	1	AI_{13}
14	1	1	1	0	AI_{14}
15	1	1	1	1	AI_{15}

Table 4 Function Select

PC	SC	Function	GS	(G0, G1)
0	0	10 bit AD CONV.	0	DISABLE
			1	ENABLE*
	1	8 bit AD CONV.	0	DISABLE
			1	ENABLE*
1	x	PROG. COMP (8 bit)	x	DISABLE

x = Do not care
* = See Table 6
[NOTE] CD bit and ST bit are effective in every case.

Status & A/D Data Register (H) (R2)

This register is a 7-bit read only register that is used to store the upper 2-bit data (C8, C9), data weight (DW), data overscale (OV), programmable comparator output (PCO), busy (BSY) and interrupt request(IRQ).

(C8, C9) (Upper bit data) : These bits store upper 2-bit data measured by 10 bit length conversion.

DW bit (Data weight) : This bit indicates data weight when Auto range-switching mode is selected. This bit is set or reset when the conversion has completed. The conditions are shown in following Table.
In this mode GAINSEL output also goes "High" or "Low" on the same condition shown in Table 5.
Other status of DW bit is shown in Table 6.

OV bit (Over scale) : This bit is set when analog data is greater than or equal to reference Voltage ($V_{REF(+)}$).

PCO bit (Programmable comparator Output) : This bit indicates the result of programmable voltage comparison.
"1" → PCO $V_{Ain} > Vp$
"0" → PCO $V_{Ain} < Vp$
V_{Ain} : Analog Input Voltage to be compared
Vp : Programmed Voltage (R4)

BSY bit (Busy) : This bit indicates that the ADU is now under conversion.

IRQ bit (Interrupt Request) : This bit is set when the A/D conversion has completed and cleared by reading the R3.

A/D Data Register (L) (R3)

This register is an 8-bit read-only register that is used to store the lower 8 bits data of 10-bit conversion or full 8 bits data of the 8-bit conversion.

PC Data Register (R4)

This register is an 8-bit write-only register prepared for Programmable Voltage comparison. Stored data is converted to digital voltage, and compared with analog input to be measured. The result of comparison is set into PCO bit.

Table 5 Data Weight (DW) Set or Reset Condition

Mode \ Condition	Set ("1")	Reset ("0")
Auto Range-Switching (x2)	$V_{Ain} < \frac{410}{1024} \cdot V_{REF(+)}$	$V_{Ain} > \frac{410}{1024} \cdot V_{REF(+)}$
Auto Range-Switching (x4)	$V_{Ain} < \frac{206}{1024} \cdot V_{REF(+)}$	$V_{Ain} > \frac{206}{1024} \cdot V_{REF(+)}$

V_{Ain} : Analog Input Voltage to be measured
$V_{REF(+)}$: Voltage Applied to REF(+)

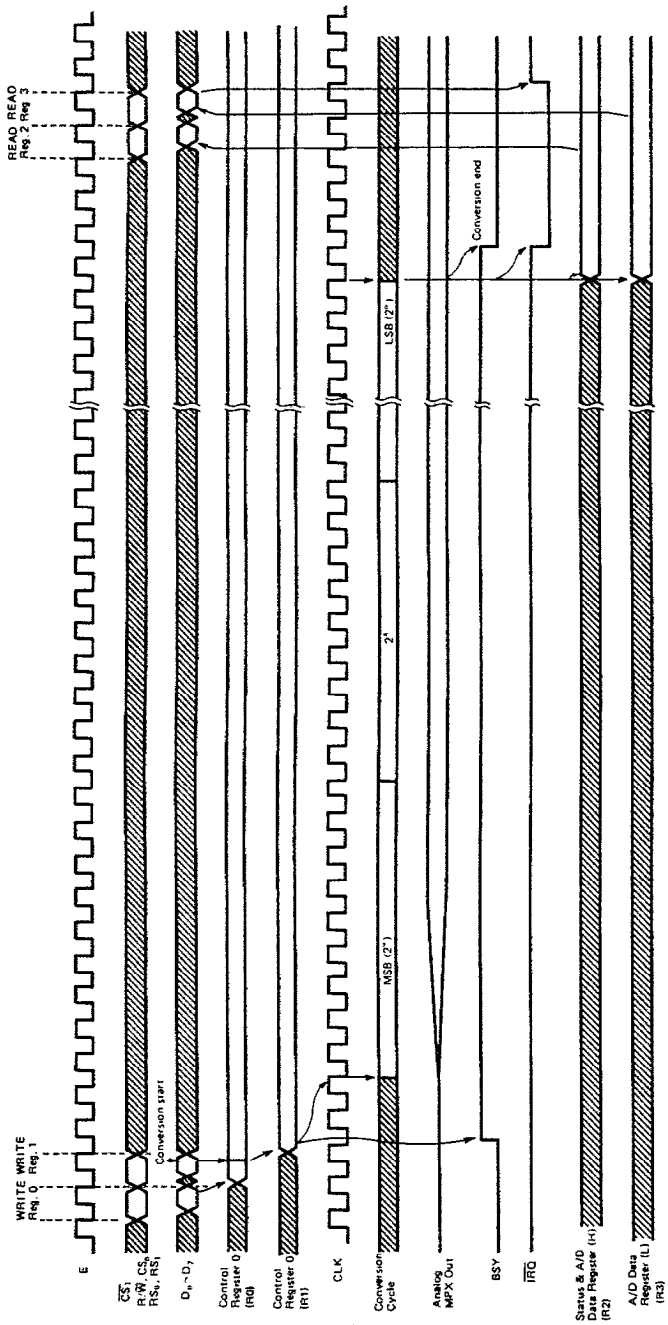
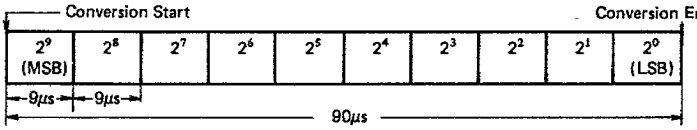


Figure 13 A/D Conversion Timing Chart (Basic Sequence)

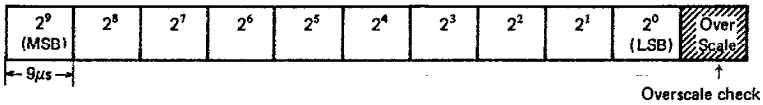
- **A/D Conversion and PC sequence** (t_{cyc}=1μs)

10 bits A/D Conversion

1) Basic Sequence (SC = "0", ST = "0", GS = "0")

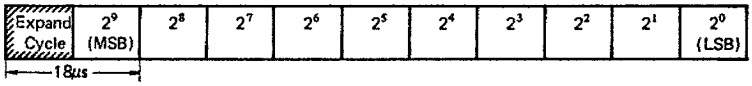


2) Basic Sequence (When overscale is detected)



Overscale check Cycle (Analog Input is compared with $V_{REF(+)}$.)

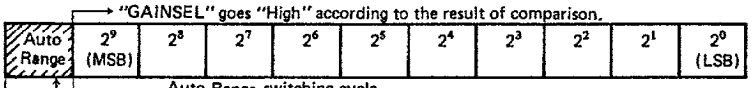
3) Expanded Sequence (SC = "0", ST = "1", GS = "0")



MSB cycle is expanded to compensate external amplifier's settling delay.

4) Auto Range-Switching Control Sequence

SC = "0", ST = "0", GS = "1", G0 = "0", G1 = "1"
or
G0 = "1", G1 = "0"

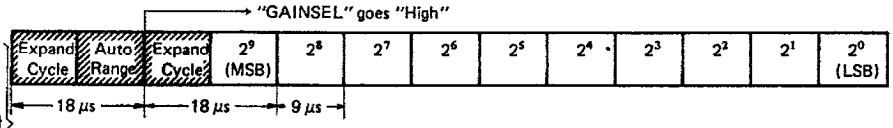


Auto Range-switching cycle (Analog Input is compared with 1/2 $V_{REF(+)}$ or 1/4 $V_{REF(+)}$ at this cycle)

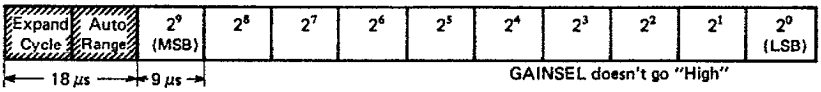
5) Auto Range-Switching & Expansion Control Sequence

SC = "0", ST = "1", GS = "1", G0 = "0", G1 = "1"
or
G0 = "1", G1 = "0"

a) Analog Input < 1/2 $V_{REF(+)}$ or 1/4 $V_{REF(+)}$



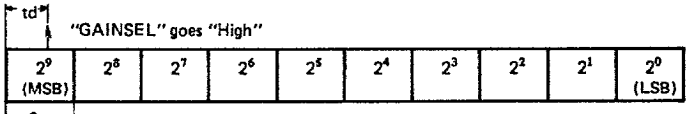
b) Analog Input > 1/2$V_{REF(+)}$ or 1/4$V_{REF(+)}$



GAINSEL doesn't go "High"

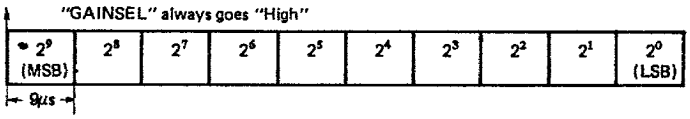
6) Sample & Hold Control Sequence

SC = "0", ST = "0", GS = "1", G0 = "0", G1 = "0"

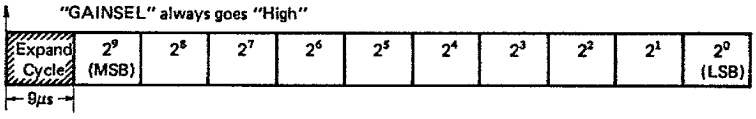


t_d = 5.5μs + t_{GSD1} or t_{GSD2}

7) Programmable Gain Control Sequence
(SC = "0", ST = "0", GS = "1", G0 = "1", G1 = "1")

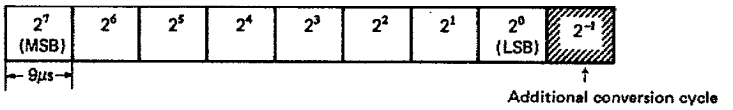


8) Programmable Gain & Expansion Control Sequence
(SC = "0", ST = "1", GS = "1", G0 = "1", G1 = "1")

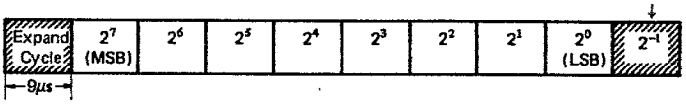


8 Bit A/D Conversion

1) Basic Sequence
(SC = "1", ST = "0", GS = "0")



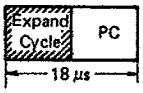
2) Expanded Sequence
(SC = "1", ST = "1", GS = "0")



Programmable Voltage Comparison

1) Basic Sequence
(PC = "1", ST = "0")

2) Expanded Sequence
(PC = "1", ST = "1")



■ HOW TO USE THE ADU

• Functions of GAINSEL

The ADU is equipped with programmable GAINSEL output signal. By using GAINSEL output and external circuit, the ADU is able to implement following control.

1) Auto Range-Switching (Auto Gain) Control
2) Programmable Gain control
3) Sample & Hold control

GAINSEL output is controlled by Mode Select bit (G0, G1) when GAINSEL enable bit (GS) is "1".

Table 6 GAINSEL Control

GS	G1	G0	GAINSEL	Control Mode	DW
0	x	x	"Low"	Normal Use (GAINSEL is not used)	0
1	0	0	"High"	Sample & Hold control	0
1	0	1	*	Auto Range Switching x 2 control	**
1	1	0	*	Auto Range Switching x 4 control	**
1	1	1	"High"	Programmable Gain control	1

* GAINSEL goes "High" or "Low" according to the condition shown in Table 5.
** See, Table 5.

How to Control External Circuit

(1) Sample & Hold Control (G1=0, G0=0)

An example of Sample & Hold circuit is shown in Fig. 14. When ADU is set in Sample & Hold Control Mode, GAINSEL becomes "High" level on conversion and controls the data holding.

(2) Automatic Range Switching Control (G1=0, G0=1 or G1=1, G0=0)

The GAINSEL signal controls the external amplifier which can change the ratio of voltage amplification. (GAIN: 1 → 2 times or 1 → 4 times). Fig. 15 shows Automatic Range Switching Control. In this case, when the input voltage is lower than 206/1024 $V_{REF(+)}$, GAINSEL becomes "High" level. This makes the GAIN of the amplifier change from 1 to 4 times, and 4 times value of the input voltage is A/D converted. Using this function even if an input signal is small, it is possible to execute A/D conversion in nearly full scale. In this mode, when GAINSEL signal becomes "High", DW bit becomes "1" to show the range switching is in a progress.

(3) Programmable GAIN Control (G1=1, G0=1)

The GAINSEL signal is used for controlling the external amplifier of any GAIN which is fit to the system.

In this mode, GAINSEL always becomes "High" at the beginning of A/D conversion, so the change of range is controlled by GS bit. Converted data need to be corrected in software in accordance with GAIN of the amplifier.

This mode is effective in the case of converting very small input voltage.

(Note) Refer to "ADU Function Sequence" (A/D Conversion and PC Sequence) for the timing in which GAINSEL signal becomes "High". GAINSEL signal becomes "Low" in accordance with "1" → "0" change of BSY bit. Refer to Fig. 13.

x1 Sample & Hold

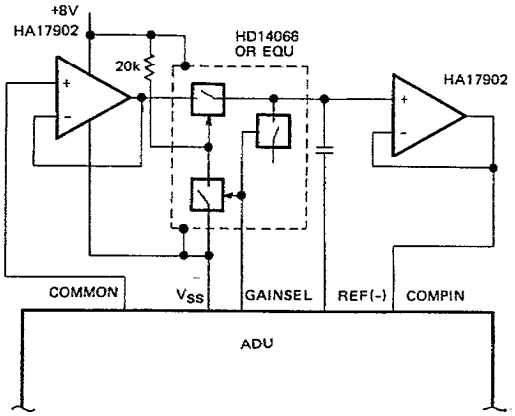


Figure 14 Sample & Hold Circuit

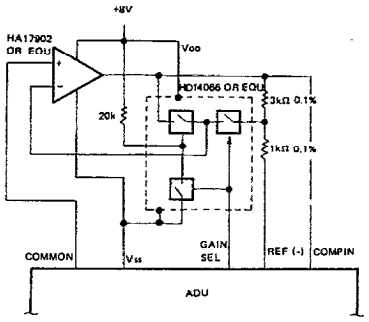
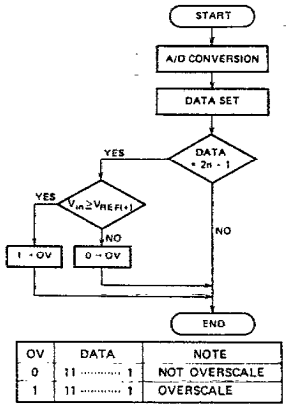


Figure 15 Pre-amplifier Circuit
(x1, x4 Auto-Range Switching)

- **Overscale Check**

ADU is equipped with hardware overscale detection function. The overscale detection is performed automatically when the result of A/D conversion is 2^n-1 (all bits = 1). When analog input V_{Ain} is higher than $V_{REF(+)}$, overscale bit (OV) is set to "1". The definition of the overscale is illustrated in Fig. 17. And the flow of overscale check is shown in Fig. 16.



OV	DATA	NOTE
0	11 1	NOT OVERSCALE
1	11 1	OVERSCALE

Figure 16 Overscale Check Flow

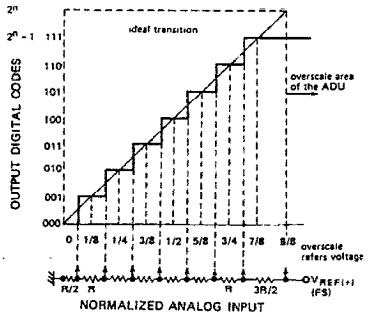


Figure 17 Definition ADU's Overscale

- **Usage of the PC**

The ADU has a programmable threshold voltage comparator (PC) function. The threshold voltage is pre-setable from 0V to 5V range with 8 bit resolution. The comparator's output is stored into PCO bit at the end of comarison.

The programmable voltage comparison time is so short that the interrupt is not requested at this mode. The end of comparison needs to be confirmed by reading the 1→0 transition of the BSY bit in R2.

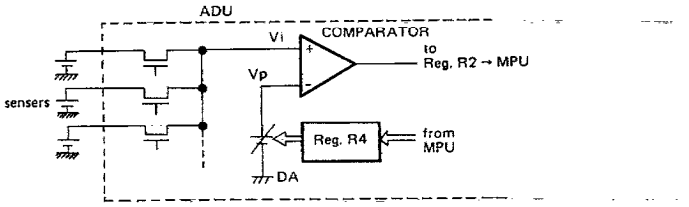
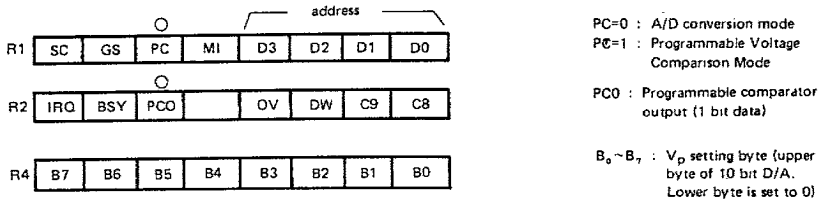


Figure 18 Function Diagram of the PC



PC=0 : A/D conversion mode
PC=1 : Programmable Voltage Comparison Mode

PCO : Programmable comparator output (1 bit data)

B_0~B_7 : V_P setting byte (upper byte of 10 bit D/A. Lower byte is set to 0)

Figure 19 Registers of the PC Mode

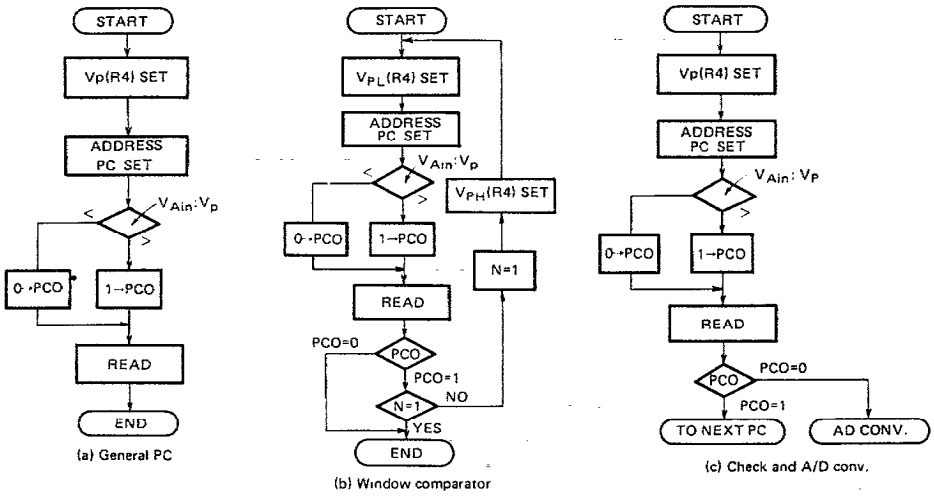
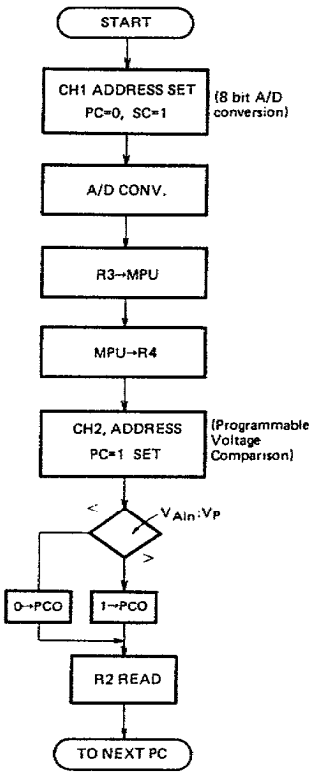


Figure 20 PC Application Flow Chart Examples



(d) Voltage Comparison between two channels.

Figure 20 PC Application Flow Chart Examples (continued)

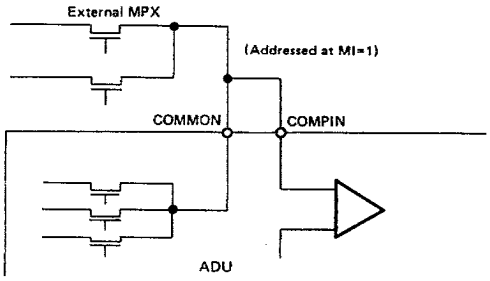
- **How to use MI bit**

MI bit (R1) functions as follows.

MI = 1: Internal MPX channel is inhibited in order to use attached external MPX channel.

MI = 0: Internal MPX channel is enabled.

MI bit used to select either of External MPX and Internal MPX. External MPX is connected as follows.



[NOTE] When external MPX is used as the way figure 20, 1 dammy AD conversion or PC at MI=1 should be performed.

Figure 21 How to use External MPX

- **EXAMPLE OF APPLIED CIRCUIT OF THE ADU**

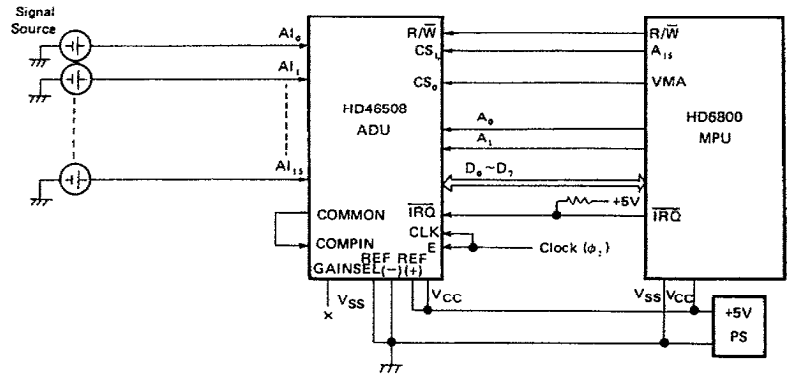


Figure 22 Single ADU System

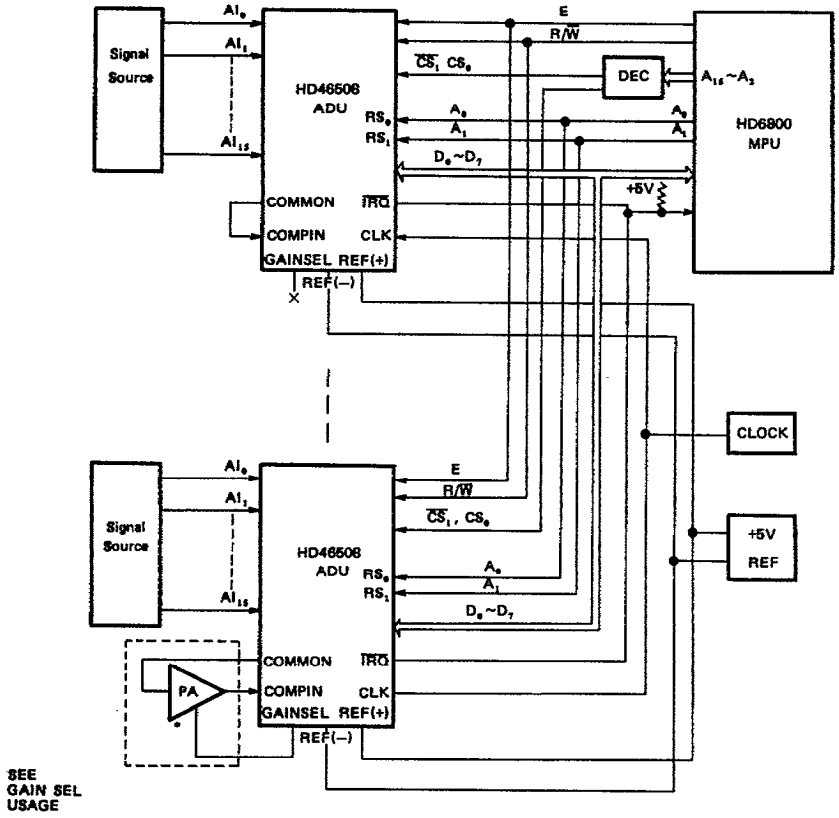


Figure 23 Multi ADU System

■ DEFINITIONS OF ACCURACY

Definitions of accuracy applyed to HD46508 are as follows.

(1) Resolution . . . The number of output binary digit.

(2) Offset Error . . . The difference between actual input voltage and ideal input voltage for the first transition. (when digital output code is changed from 000 . . . 00 to 000 . . . 01.)

(3) Full Scale Error . . . The difference between actual input voltage and ideal input voltage for the final transition. (when digital output code is changed from 111 . . . 10 to 111 . . . 11.)

(4) Quantizing Error . . . Error equipped in A/D converter inherently. Always ±½ LSB is applied.

(5) Non-linearity Error . . . The maximum deviation of the actual transfer line from an ideal straight line. This error doesn't include Quantizing Error, Offset, or Full Scale Errors.

(6) Absolute Accuracy . . . The deviation of the digital output code from an analog input voltage. Absolute accuracy includes all of (2), (3), (4), (5).

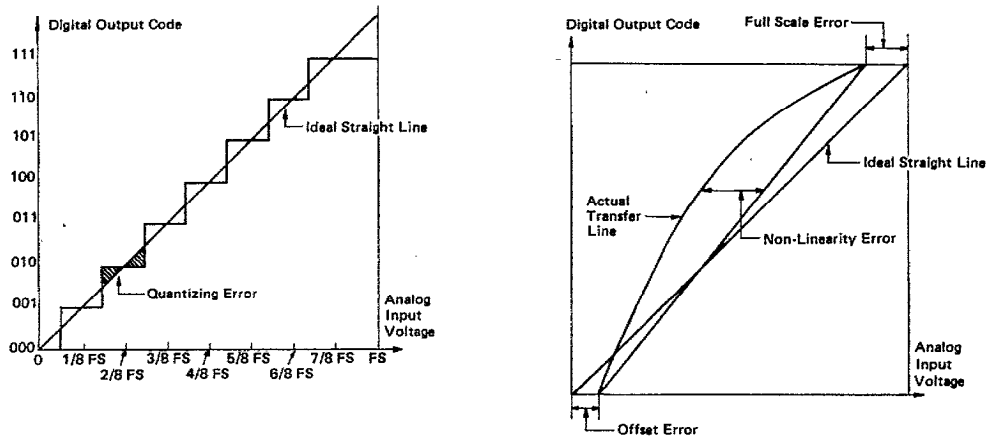


Figure 24 Definition of Accuracy

HD146818

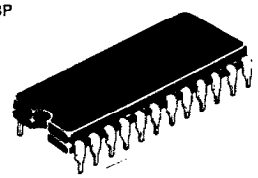
RTC (Real Time Clock Plus RAM)

The HD146818 is a HMCS6800 peripheral CMOS device which combines three unique features: a complete time-of-day clock with alarm and one hundred calendar, a programmable periodic interrupt and square-wave generator, and 50 bytes of Low-power static RAM.

This device includes HD6801, HD6301 multiplexed bus interface circuit and 8085's multiplexed bus interface as well, so it can be directly connected to HD6801, HD6301 and 8085.

The Real-Time Clock plus RAM has two distinct uses. First, it is designed as battery powered CMOS part including all the common battery backed-up functions such as RAM, time, and calender. Secondly, the HD146818 may be used with a CMOS microprocessor to relieve the software of timekeeping workload and to extend the available RAM of an MPU such as the HD6301.

HD146818P



(DP-24)

HD146818FP

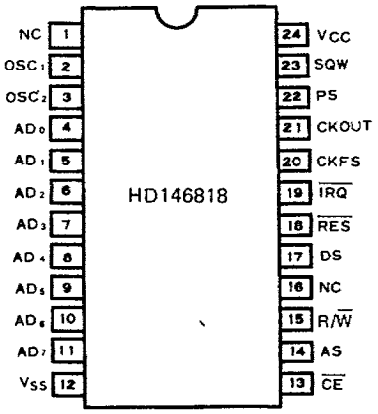
(FP-24)

The Flat Package product is under development.

■ FEATURES

- Time-of-Day Clock and Calendar
  - Counts Seconds, Minutes, and Hours of the Day
  - Counts Days of Week, Date, Month, and Year
- Binary or BCD Representation of Time, Calendar, and Alarm
- 12- or 24 Hour Clock with AM and PM in 12-Hour Mode
- Automatic End of Month Recognition
- Automatic Leap Year Compensation
- Interfaced with Software as 64 RAM Locations
  - 14 Bytes of Clock and Control Register
  - 50 Bytes of General Purpose RAM
- Three Interrupt are Separately Software Maskable and Testable
  - Time-of-Day Alarm, Once-per-Second to Once-per-Day
  - Periodic Rates from 30.5μs to 500ms
  - End-of-Clock Update Cycle
- Programmable Square-Wave Output Signal
- Three Time Base Input Options
  - 4.194304 MHz
  - 1.048576 MHz
  - 32.768 kHz
- Clock Output May be used as Microprocessor Clock Input
  - At Time Base Frequency ÷4 or ÷1
- Multiplexed Bus Interface Circuit of HD6801, HD6301 and 8085
- Low-Power, High-Speed, High-Density CMOS
- Battery Backed-up Operation
- Motorola MC146818 Compatible

■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{CC} *	-0.3 ~ +7.0	V
Input Voltage	V_{in} *	-0.3 ~ +7.0	V
Operating Temperature	T_{opr}	0 ~ +70	°C
Storage Temperature	T_{stg}	-55 ~ +150	°C

* With respect to V_{SS} (SYSTEM GND)

(NOTE) Permanent LSI damage may occur if maximum rating are exceeded. Normal operation should be under recomended operating condition. If these conditions are exceeded, it could affect reliability of LSI.

■ RECOMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC} *	4.5	5.0	5.25	V
Input Voltage	V_{IL} *	-0.3	–	0.7	V
	V_{IH} *	V_{CC}-1.0	–	V_{CC}	V
Operating Temperature	T_{opr}	0	25	70	°C

* With respect to V_{SS} (SYSTEM GND)
(NOTE) Refer to Battery Backed-up Electrical characteristics.

■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS (V_{CC} = 4.5 ~ 5.25V, V_{SS} = 0V, Ta = 0 ~ +70°C, unless otherwise noted.)

Item		Symbol	Test Condition	min	typ	max	Unit
Input "High" Voltage	AD_0~AD_7, $\overline{CE}$, AS, R/$\overline{W}$, DS, CKFS, PS	V_{IH}		V_{CC}-2.0	–	V_{CC}	V
	$\overline{RES}$			V_{CC}-1.0	–	V_{CC}	
	OSC_1			V_{CC}-1.0	–	V_{CC}	
Input "Low" Voltage	AD_0~AD_7, $\overline{CE}$, AS, R/$\overline{W}$, DS, CKFS, PS	V_{IL}		-0.3	–	0.7	V
	$\overline{RES}$			-0.3	–	0.8	
	OSC_1			-0.3	–	0.8	
Input Leakage Current	OSC_1, $\overline{CE}$, AS, R/$\overline{W}$, DS, $\overline{RES}$, CKFS, PS	$\lvert I_{in}\rvert$		–	–	2.5	μA
Three-state (off state) Input Current	AD_0~AD_7	$\lvert I_{TSI}\rvert$		–	–	10	μA
Output Leakage Current	$\overline{IRQ}$	I_{LOH}		–	–	10	μA
Output "High" Voltage	AD_0~AD_7	V_{OH}	I_{OH} = -1.6 mA	4.1	–	–	V
	SQW, CKOUT						
	AD_0~AD_7		I_{OH} <-- 10 μA	V_{CC}-0.1	–	–	V
	SQW, CKOUT						
Output "Low" Voltage	AD_0~AD_7	V_{OL}	I_{OL} = 1.6 mA	–	–	0.5	V
	CKOUT		I_{OL} = 1.6 mA				
	$\overline{IRQ}$, SQW		I_{OL} = 1.6 mA				
Input Capacitance	AD_0~AD_7	C_{in}	V_{in} = 0V Ta = 25°C f = 1 MHz	–	–	12.5	pF
	All inputs except AD_0~AD_7			–	–	12.5	pF
Output Capacitance	SQW, CKOUT, $\overline{IRQ}$	C_{out}		–	–	12.5	pF
Supply Current (MPU Read/Write operating)	Crystal Oscillation: f_{OSC} = 4 MHz	I_{CC} *	V_{CC} = 5.0V SQW: disable CKOUT = fosc (No Load) t_{cyc} = 1 μs Circuit: Fig. 11 Parameter: Table 1	–	–	10	mA
	f_{OSC} = 1 MHz			–	–	7	
	f_{OSC} = 32 kHz			–	–	5	
Supply Current ** (MPU not operating)	f_{OSC} = 4 MHz			–	–	5	mA
	f_{OSC} = 1 MHz			–	–	2	
	f_{OSC} = 32 kHz			–	300	500	μA
Supply Current (MPU Read/Write operating)	External Clock: f_{OSC} = 4 MHz	I_{CC} *	V_{CC} = 5.0V SQW: disable CKOUT = fosc (No Load) OSC_2: open t_{cyc} = 1 μs Circuit: Fig. 17	–	–	10	mA
	f_{OSC} = 1 MHz			–	–	7	
	f_{OSC} = 32 kHz			–	–	5	
Supply Current ** (MPU not operating)	f_{OSC} = 4 MHz			–	–	4	mA
	f_{OSC} = 1 MHz			–	–	1	
	f_{OSC} = 32 kHz			–	60	100	μA

* Supply current of HD146818 is defined as the value when the time-base frequency to be used is programmed into Register A. When power is turned on, these bits are unfixed, so there is a case that current more than the above specification may flow. Please never fail to set the time-base frequency after turning on power supply.

** $V_{IH\ min}$ = V_{CC}-0.2V
$V_{IL\ max}$ = V_{SS}+0.2V

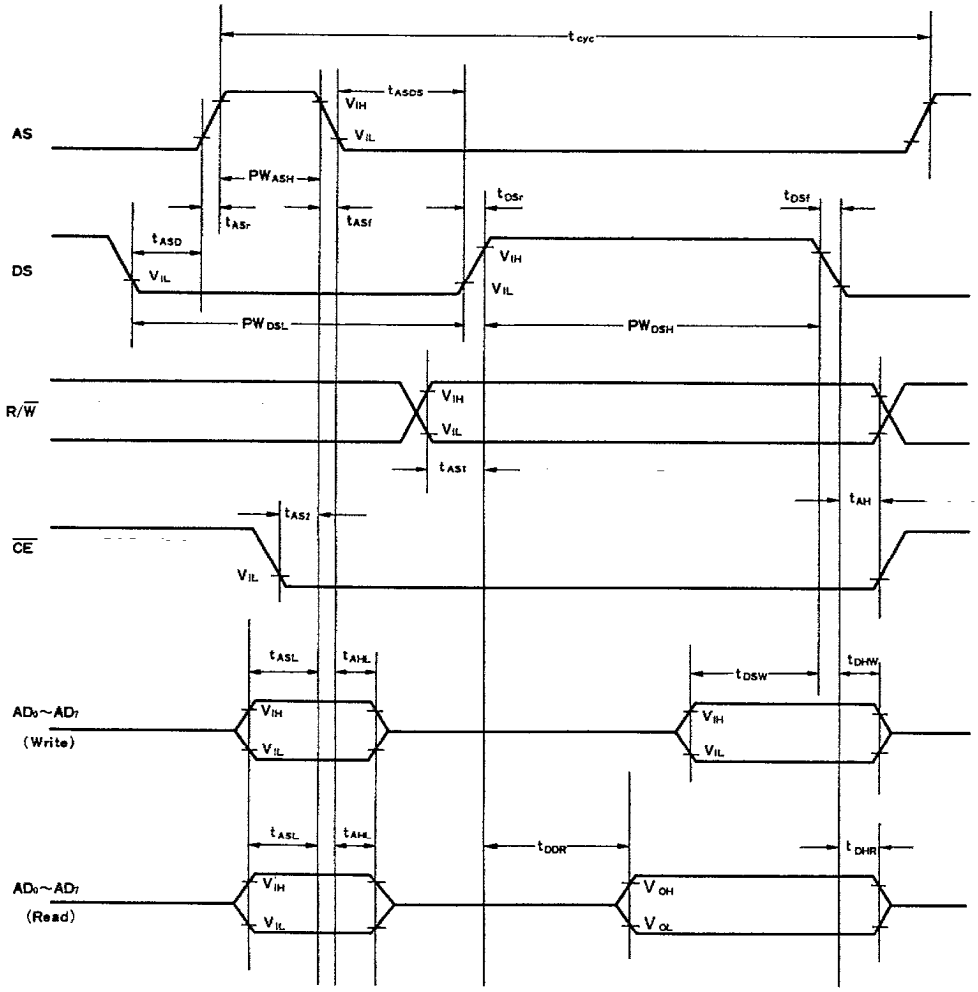
- **AC CHARACTERISTICS (V_{CC} = 4.5 ~ 5.25V, V_{SS} = 0V, Ta = 0 ~ +70°C, unless otherwise noted.)**

BUS TIMING

Item	Symbol	min	typ	max	Unit
Cycle Time	t_{cyc}	953	–	–	ns
Pulse Width, AS/ALE "High"	PW_{ASH}	100	–	–	ns
AS Rise Time	t_{ASr}	–	–	30	ns
AS Fall Time	t_{ASf}	–	–	30	ns
Delay Time DS/E to AS/ALE Rise	t_{ASD}	40	–	–	ns
DS Rise Time	t_{DSr}	–	–	30	ns
DS Fall Time	t_{DSf}	–	–	30	ns
Pulse Width, DS/E Low or $\overline{RD}/\overline{WR}$ "High"	PW_{DSH}	325	–	–	ns
Pulse Width, DS/E High or $\overline{RD}/\overline{WR}$ "Low"	PW_{DSL}	300	–	–	ns
Delay Time, AS/ALE to DS/E Rise	t_{ASDS}	90	–	–	ns
Address Setup Time (R/$\overline{W}$)	t_{AS1}	15	–	–	ns
Address Setup Time ($\overline{CE}$)	t_{AS2}	55	–	–	ns
Address Hold Time (R/$\overline{W}$, $\overline{CE}$)	t_{AH}	10	–	–	ns
Muxed Address Valid Time to AS/ALE Fall	t_{ASL}	50	–	–	ns
Muxed Address Hold Time	t_{AHL}	20	–	–	ns
Peripheral Data Setup Time	t_{DSW}	195	–	–	ns
Write Data Hold Time	t_{DHW}	0	–	–	ns
Peripheral Output Data Delay Time From DS/E or $\overline{RD}$	t_{DDR}	–	–	220	ns
Read Data Hold Time	t_{DHR}	10	–	–	ns

CONTROL SIGNAL TIMING

Item		Symbol	min	typ	max	Unit
Oscillator Startup	1 MHz, 4 MHz	t_{RC}	–	–	100	ms
	32 kHz		–	–	1000	
Reset Pulse Width		t_{RWL}	5.0	–	–	μs
Reset Delay Time		t_{RLH}	5.0	–	–	μs
Power Sense Pulse Width		t_{PWL}	5.0	–	–	μs
Power Sense Delay Time		t_{PLH}	5.0	–	–	μs
$\overline{IRQ}$ Release from DS		t_{IRDS}	–	–	2.0	μs
$\overline{IRQ}$ Release from $\overline{RES}$		t_{IRR}	–	–	2.0	μs
VRT Bit Delay		t_{VRTD}	–	–	2.0	μs



(NOTE) $V_{IH} = V_{OH} = V_{CC}-2.0V$
$V_{IL} = 0.7V$
$V_{OL} = 0.5V$

Figure 1 Bus Read, Write Timing (6801 Family)

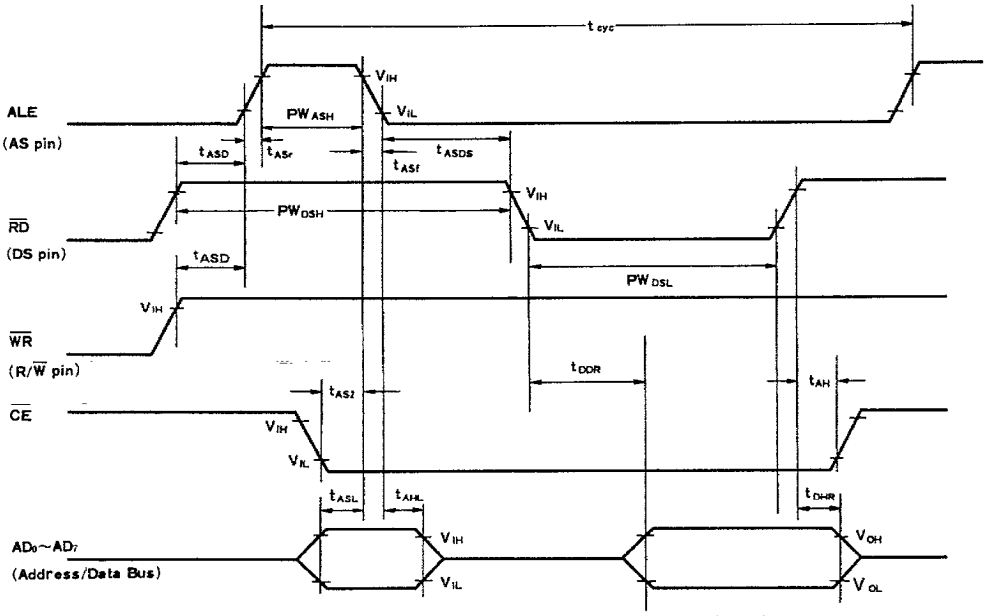


Figure 2 Read Timing (8085 Family)

(NOTE) $V_{IH} = V_{OH} = V_{CC}-2.0V$
$V_{IL} = 0.7V, V_{OL} = 0.5V$

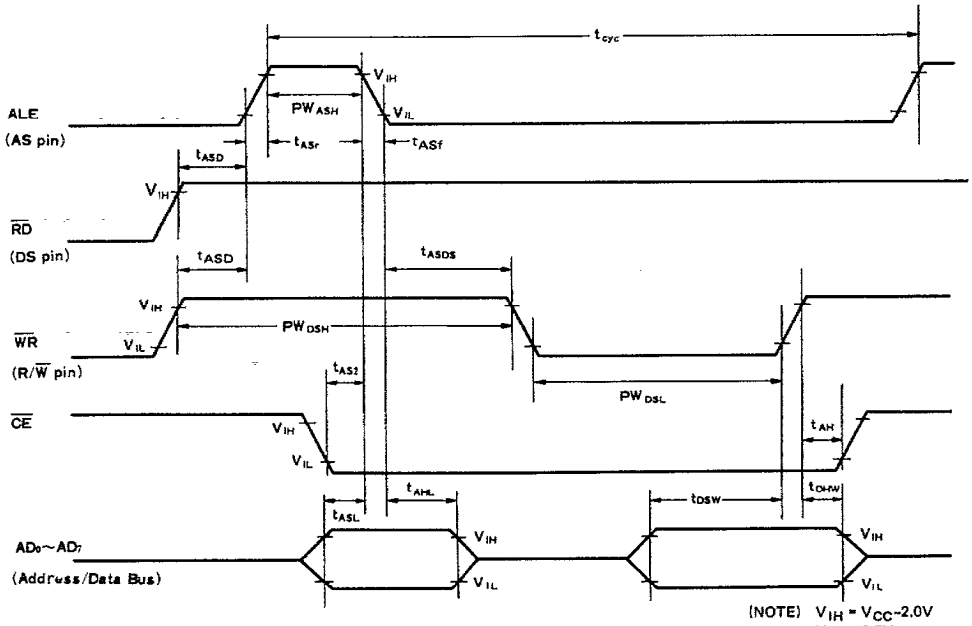


Figure 3 Write Timing (8085 Family)

(NOTE) $V_{IH} = V_{CC}-2.0V$
$V_{IL} = 0.7V$

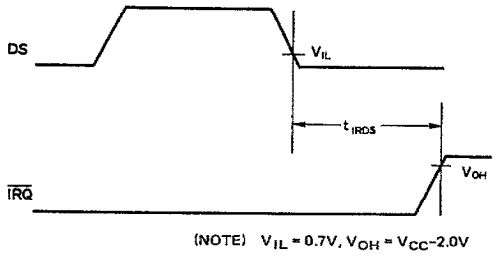


Figure 4 $\overline{IRQ}$ Release Delay (from DS)

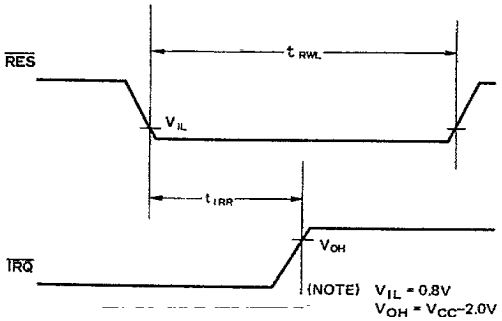
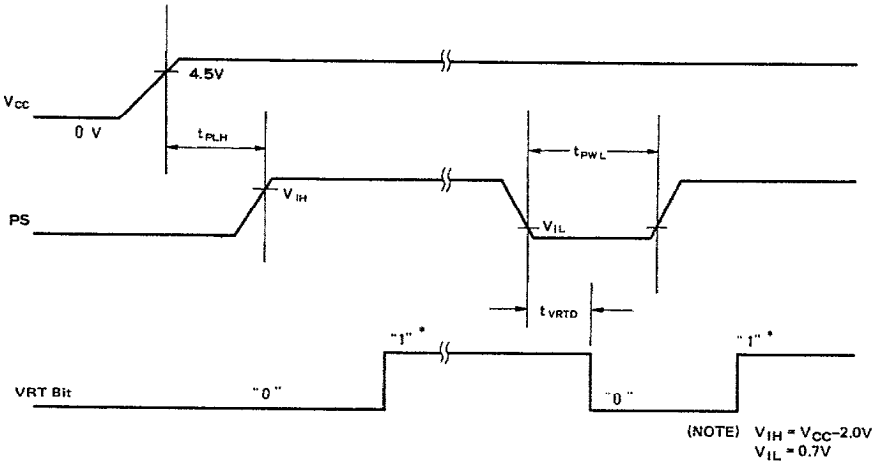


Figure 5 $\overline{IRQ}$ Release Delay (from $\overline{RES}$)



* The VRT bit is set to a "1" by reading control register #D. There is no additional way to clear the VRT bit.

Figure 6 VRT Bit Clear Timing

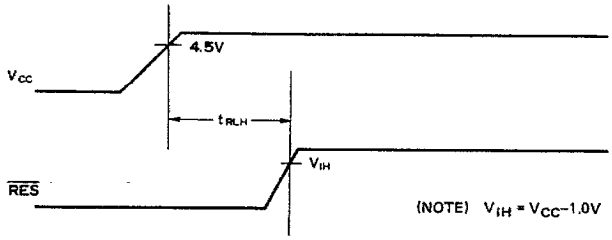


Figure 7 $\overline{RES}$ Release Delay

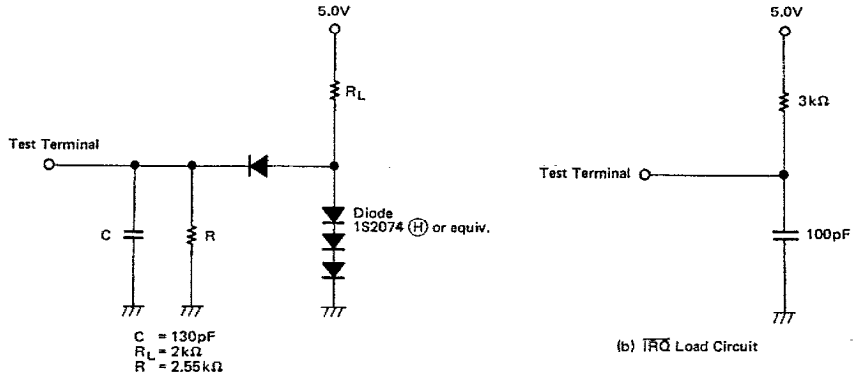


Figure 8 Test Load

■ BATTERY BACKED-UP OPERATION

• DEFINITION OF BATTERY BACKED-UP OPERATION

Active functions
(1) Clock function
(2) Retention of RAM data
(3) $\overline{RES}$, $\overline{IRQ}$, CKFS, CKOUT, PS, SQW functions

Inactive functions
(1) Data bus read/write operation

• BATTERY BACKED-UP ELECTRICAL CHARACTERISTICS (V_{SS} = 0V, T_a = 0 ~ +70°C, unless otherwise noted.)

Item		Symbol	Test Condition		min	typ	max	Unit
Supply Voltage		V_{CCL}			2.7	–	4.5	V
Supply Current	Crystal Oscillation	I_{CCL}*	V_{CCL} = 3.0V SQW : disable CKOUT: fosc (No load)	4MHz	–	–	600	μA
				1MHz	–	–	350	μA
				32kHz	–	50	100	μA
	External Clock		V_{CCL} = 3.0V SQW : disable CKOUT: fosc (No load)	4MHz	–	–	500	μA
				1MHz	–	–	150	μA
				32kHz	–	30	70	μA
Battery Backed-up Transit Setup Time		t_{CE}	Fig. 9		0	–	–	ns
Operation Recovery Time		t_R			t_{cyc}	–	–	ns
Supply Voltage Fall Time		t_{Pf}			300	–	–	μs
Supply Voltage Rise Time		t_{Pr}			300	–	–	μs
Input "High" Voltage		V_{IHL}	V_{CCL} = 2.7V ~ 3.5V	$\overline{CE}$, PS CKFS	0.7×V_{CCL}	–	V_{CCL}	V
			V_{CCL} = 3.5V ~ 4.5V		2.5	–	V_{CCL}	V
				$\overline{RES}$	0.8×V_{CCL}	–	V_{CCL}	V
				OSC_1	0.8×V_{CCL}	–	V_{CCL}	V
Input "Low" Voltage		V_{ILL}		CKFS, PS	-0.3	–	0.5	V
				$\overline{RES}$	-0.3	–	0.5	V
				OSC_1	-0.3	–	0.5	V
Output "High" Voltage		V_{OHL}	I_{OH} = -800μA	SQW, CKOUT	0.8×V_{CCL}	–	–	V
Output "Low" Voltage		V_{OLL}	I_{OL} = 800μA	SQW, CKOUT	–	–	0.5	V
				$\overline{IRQ}$	–	–	0.5	V

* The time-base frequency to be used needs to be chosen in Register A.

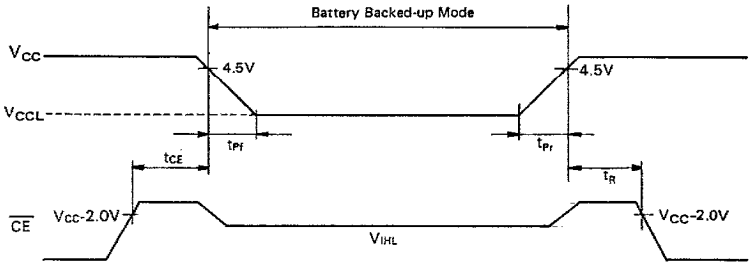


Figure 9 Battery Backed-up Timing

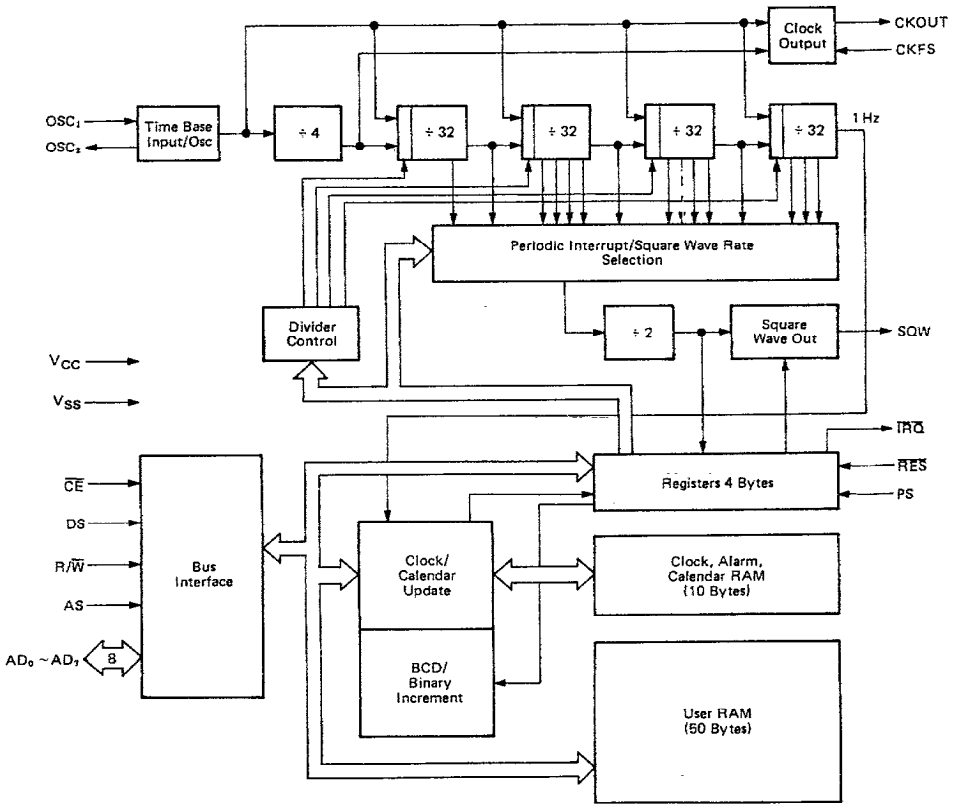


Figure 10 Block Diagram

■ CRYSTAL OSCILLATION CIRCUIT

The on-chip oscillator is designed for a parallel resonant crystal at 4.194304 MHz or 1.048576 MHz or 32.768 kHz frequencies. The crystal connections are shown in Figure 11.

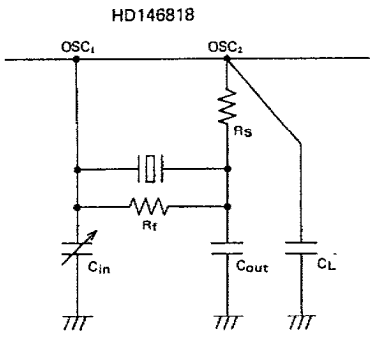


Figure 11 Crystal Oscillator Connection

Table 1 Oscillator Circuit Parameters

Parameter \ fosc	4.194304 MHz	1.048576 MHz	32.768 kHz
R_S	–	–	150 kΩ
R_f	150 kΩ	150 kΩ	5.6 MΩ
C_{in}	22 pF	33 pF	15 pF
C_{out}	22 pF	33 pF	33 pF
C_L	–	–	33 pF
CI	80 Ω (max)	700 Ω (max)	40 kΩ (max)

(NOTE) 1. R_S, C_L are used for 32.768 kHz only.
2. Capacitance (C_{in}) should be adjusted to accurate frequency. Parameters listed above are applied to the supply current measurement (See table of DC CHARACTERISTICS).
3. CI: Crystal Impedance

■ NOTE FOR BOARD DESIGN OF THE OSCILLATION CIRCUIT

In designing the board, the following notes should be taken when the crystal oscillator is used.

(1) Crystal oscillator, load capacity C_{in}, C_{out}, C_L and R_f, R_S must be placed near the LSI as much as possible.
[Normal oscillation may be disturbed when external noise is induced to pin 2 and 3.]

(2) Pin 3 signal line should be wired apart from pin 4 signal line as much as possible. Don't wire them in parallel, or normal oscillation may be disturbed when this signal is feedbacked to OSC_1.

(3) A signal line or a power source line must not cross or go near the oscillation circuit line as shown in the right figure to prevent the induction from these lines and perform the correct oscillation. The resistance among OSC_1, OSC_2 and other pins should be over 10MΩ.

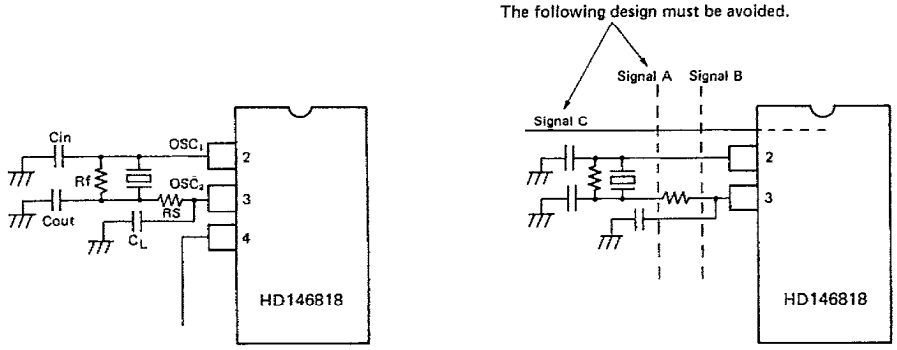


Figure 12 Note for Board Design of the Oscillation Circuit

■ INTERFACE CIRCUIT FOR HD6801, HD6301 AND 8085 PROCESSOR

HD146818 has a new interface circuit which permits the HD146818 to be directly interfaced with many type of multiplexed bus microprocessor such as HD6801, HD6301 and 8085 etc.

Figure 13 shows the bus control circuit. This circuit automatically selects the processor type by using AS/ASE to latch the state of DS/$\overline{RD}$ pin. Since DS is always "Low" and $\overline{RD}$ is always "High during AS/ALE, the latch automatically indicates which processor type is connected.

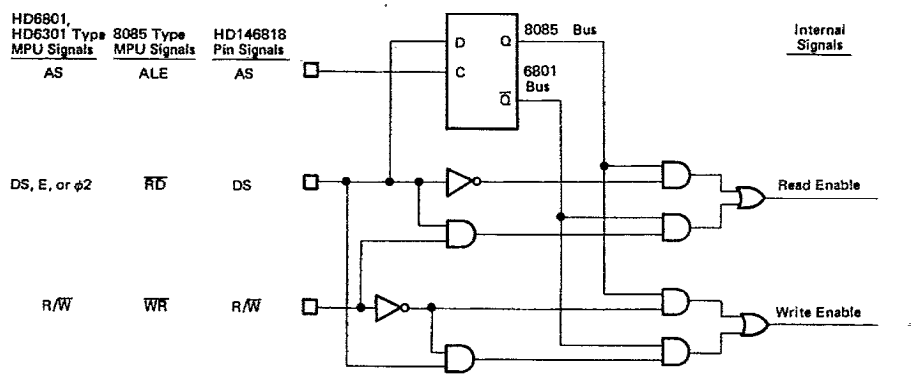


Figure 13 Functional Diagram of the Bus Control Circuit

■ ADDRESS MAP

Figure 14 shows the address map of the HD146818. The memory consists of 50 general purpose RAM bytes, 10 RAM bytes which normally contain the time, calendar, and alarm data, and four control and status bytes. All 64 bytes are directly readable and writable by the processor program except Registers C and D which are read only. Bit 7 of Register A and the seconds byte are also read only. Bit 7, of the second byte, always reads "0". The contents of the four control and status registers are described in the Register section.

• Time, Calendar, and Alarm Locations

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar, and alarm by writing to these RAM locations. The contents of the 10 time, calendar, and alarm byte may be either binary or binary-coded decimal (BCD).

Before initializing the internal registers, the SET bit in Register B should be set to a "1" to prevent time/calendar updates from occurring. The program initializes the 10 locations in the selected format (binary or BCD), then indicates the format in the data mode (DM) bit of Register B. All 10 time, calendar, and alarm bytes must use the same data mode, either binary or BCD. The SET bit may now be cleared to allow updates. Once initialized the real-time clock makes all updates in the selected data mode. The data mode cannot be changed without reinitializing the 10 data bytes.

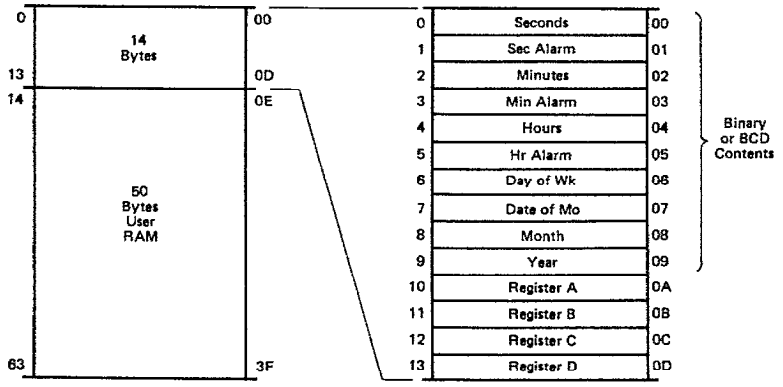


Figure 14 Address Map

Table 2 shows the binary and BCD formats of the 10 time, calendar, and alarm locations. The 24/12 bit in Register B establishes whether the hour locations represent 1-to-12 or 0-to-23. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected the high-order bit of the hours byte represents PM when it is a "1".

The time, calendar, and alarm bytes are not always accessable by the processor program. Once-per-second the 10 bytes are switched to the update logic to be advanced by one second and to check for an alarm condition. If any of the 10 bytes are read at this time, the data outputs are undefined. The update lockout time is 248 μs at the 4.194304 MHz and 1.048567 MHz time bases and 1948 μs for the 32.768 kHz time base. The Update Cycle section shows how to accommodate the update cycle in the processor program.

The three alarm bytes may be used in two ways. When the program inserts an alarm time in the appropriate hours, minutes, and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is "1". The alternate usage is to insert a "don't care" state in one or more of three alarm bytes. The "don't care" code is any hexadecimal byte from C0 to FF. That is, the two most-significant bits of each byte, when set to "1", create a "don't care" situation. An alarm interrupt each hour is created with a "don't care" code in the hours alarm location. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

Table 2 Time, Calendar, and Alarm Data Modes

Address Location	Function	Decimal Range	Range		Example*	
			Binary Data Mode	BCD Data Mode	Binary Data Mode	BCD Data Mode
0	Seconds	0~59	$00~$3B	$00~$59	15	21
1	Seconds Alarm	0~59	$00~$3B	$00~$59	15	21
2	Minutes	0~59	$00~$3B	$00~$59	3A	58
3	Minutes Alarm	0~59	$00~$3B	$00~$59	3A	58
4	Hours (12 Hour Mode)	1~12	$01~$0C (AM) and $81~$8C (PM)	$01~$12 (AM) and $81~$92 (PM)	05	05
	Hours (24 Hour Mode)	0~23	$00~$17	$00~$23	05	05
5	Hours Alarm (12 Hour Mode)	1~12	$01~$0C (AM) and $81~$8C (PM)	$01~$12 (AM) and $81~$92 (PM)	05	05
	Hours Alarm (24 Hour Mode)	0~23	$00~$17	$00~$23	05	05
6	Day of the Week Sunday = 1	1~7	$01~$07	$01~$07	05	05
7	Day of the Month	1~31	$01~$1F	$01~$31	0F	15
8	Month	1~12	$01~$0C	$01~$12	02	02
9	Year	0~99**	$00~$63	$00~$99	4F	79

* Example: 5:58:21 Thursday 15th February 1979

** Set the lower two digits of year in AD. If this number is multiple of 4, update applied to leap year is excuted.

■ Static CMOS RAM

The 50 general purpose RAM bytes are not dedicated within the HD146818. They can be used by the processor program, and are fully available during the update cycle.

When time and calendar information must use battery back-up, very frequently there is other non-volatile data that must be retained when main power is removed. The 50 user RAM bytes serve the need for low-power CMOS battery-backed storage, and extend the RAM available to the program.

When further CMOS RAM is needed, additional HD146818s may be included in the system. The time/calendar functions may be disabled by holding the dividers, in Register A, in the reset state by setting the SET bit in Register B or by removing the oscillator. Holding the dividers in reset prevents interrupts or SQW output from operating while setting the SET bit allows these functions to occur. With the dividers clear, the available user RAM is extended to 59 bytes. Bit 7 of Register A, Registers C and D, and the high-order Bit of the seconds byte cannot effectively be used as general purpose RAM.

■ INTERRUPTS

The RTC plus RAM includes three separate fully automatic sources of interrupts to the processor. The alarm interrupt may be programmed to occur at rates from once-per-second to one-a-day. The periodic interrupt may be selected for rates from half-a-second to 30.517 μs. The update-ended interrupt may be used to indicate to the program that an up-date cycle is completed. Each of these independent interrupt conditions are described in greater detail in other sections.

The processor program selects which interrupts, if any, it wishes to receive. Three bits in Register B enable the three interrupts. Writing a "1" to a interrupt-enable bit permits that interrupt to be initiated when the event occurs. A "0" in the interrupt-enable bit prohibits the $\overline{IRQ}$ pin from being asserted due to the interrupt cause.

If an interrupt flag is already set when the interrupt becomes enabled, the $\overline{IRQ}$ pin is immediately activated, though the interrupt initiating the event may have occurred much earlier. Thus, there are cases where the program should clear such

earlier initiated interrupts before first enabling new interrupts.

When an interrupt event occurs a flag bit is set to a "1" in Register C. Each of the three interrupt sources have separate flag bits in Register C, which are set independent of the state of the corresponding enable bits in Register B. The flag bit may be used with or without enabling the corresponding enable bits.

In the software scanned case, the program does not enable the interrupt. The "interrupt" flag bit becomes a status bit, which the software interrogates, when it wishes. When the software detects that the flag is set, it is an indication to software that the "interrupt" event occurred since the bit was last read.

However, there is one precaution. The flag bits in Register C are cleared (record of the interrupt event is erased) when Register C is read. Double latching is included with Register C so the bits which are set are stable throughout the read cycle. All bits which are high when read by the program are cleared, and new interrupts (on any bits) are held until after the read cycle. One, two, or three flag bits may be found to be set when Register C is read. The program should inspect all utilized flag bits every time Register C is read to insure that no interrupts are lost.

The second flag bit usage method is with fully enabled interrupts. When an interrupt-flag bit is set and the corresponding interrupt-enable bit is also set, the $\overline{IRQ}$ pin is asserted "Low". $\overline{IRQ}$ is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a "1" whenever the $\overline{IRQ}$ pin is being driven "Low".

The processor program can determine that the RTC initiated the interrupt by reading Register C. A "1" in bit 7 (IRQF bit) indicates that one of more interrupts have been initiated by the part. The act of reading Register C clears all the then-active flag bits, plus the IRQF bit. When the program finds IRQF set, it should look at each of the individual flag bits in the same byte which have the corresponding interrupt-mask bits set and service each interrupt which is set. Again, more than one interrupt-flag bit may be set.

■ DIVIDER STAGES

The HD146818 has 22 binary-divider stages following the time base as shown in Figure 10. The output of the dividers is a 1 Hz signal to the update-cycle logic. The dividers are controller by three divider bus (DV2, DV1, and DV0) in Register A.

• Divider Control

The divider-control bits have three uses, as shown in Table 3. Three usable operating time bases may be selected (4.194304 MHz, 1.048576 MHz, or 32.768 kHz). The divider chain may be held reset, which allows precision setting of the time. When the divider is changed from reset to an operating time base, the first update cycle is one second later. The divider-control bits are also used to facilitate testing the HD146818.

Table 3 Divider Configurations

Time-Base Frequency	Divider Bits Register A			Operation Mode	Divider Reset	Bypass First N-Divider Bits
	DV2	DV1	DV0			
4.194304 MHz	0	0	0	Yes	–	N = 0
1.048576 MHz	0	0	1	Yes	–	N = 2
32.768 kHz	0	1	0	Yes	–	N = 7
Any	1	1	0	No	Yes	–
Any	1	1	1	No	Yes	–

(NOTE) Other combinations of divider bits are used for test purposes only.

• Square-Wave Output Selection

Fifteen of the 22 divider taps are made available to a 1-of-15 selector as shown in Figure 10. The first purpose of selecting a divider tap is to generate a square-wave output signal in the SQW pin. Four bits in Register A establish the square-wave frequency as listed in Table 4. The SQW frequency selection shares the 1-of-15 selector with periodic interrupts.

Once the frequency is selected, the output of the SQW pin may be turned on and off under program control with the square-wave enable (SQWE) bit in Register B. Altering the divider, square-wave output selection bits, or the SQW output-enable bit may generate an asymetrical waveform at the time of execution. The square-wave output pin has a number of potential uses. For example, it can serve as a frequency standard for external use, a frequency synthesizer, or could be used to generate one or more audio tones under program control.

• Periodic Interrupt Selection

The periodic interrupt allows the $\overline{IRQ}$ pin to be triggered from once every 500 ms to once every 30.517 μs. The periodic interrupt is separate from the alarm interrupt which may be output from once-per-second to once-per-day.

Table 4 shows that the periodic interrupt rate is selected with the same Register A bits which select the square-wave frequency. Changing one also changes the other. But each function may be separately enabled so that a program could switch between the two features or use both. The SQW pin is enabled by the SQWE bit. Similarly the periodic interrupt is enabled by the PIE bit in Register B.

Periodic interrupt is usable by practically all real-time systems. It can be used to scan for all forms of input from contact closures to serial receive bits or tyes. It can be used in multiplexing displays or with software counters to measure inputs, create output intervals, or await the next needed software function.

Table 4 Periodic Interrupt Rate and Square Wave Output Frequency

Rate Select Control Register 1				4.194304 or 1.048576 MHz Time Base		32.768 kHz Time Base	
RS3	RS2	RS1	RS0	Periodic Interrupt Rate t_{PI}	SQW Output Frequency	Periodic Interrupt Rate t_{PI}	SQW Output Frequency
0	0	0	0	None	None	None	None
0	0	0	1	30.517 μs	32.768 kHz	3.90625 ms	256 Hz
0	0	1	0	61.035 μs	16.384 kHz	7.8125 ms	128 Hz
0	0	1	1	122.070 μs	8.192 kHz	122.070 μs	8.192 kHz
0	1	0	0	244.141 μs	4.096 kHz	244.141 μs	4.096 kHz
0	1	0	1	488.281 μs	2.048 kHz	488.281 μs	2.048 kHz
0	1	1	0	976.562 μs	1.024 kHz	976.562 μs	1.024 kHz
0	1	1	1	1.953125 ms	512 Hz	1.953125 ms	512 Hz
1	0	0	0	3.90625 ms	256 Hz	3.90625 ms	256 Hz
1	0	0	1	7.8125 ms	128 Hz	7.8125 ms	128 Hz
1	0	1	0	15.625 ms	64 Hz	15.625 ms	64 Hz
1	0	1	1	31.25 ms	32 Hz	31.25 ms	32 Hz
1	1	0	0	62.5 ms	16 Hz	62.5 ms	16 Hz
1	1	0	1	125 ms	8 Hz	125 ms	8 Hz
1	1	1	0	250 ms	4 Hz	250 ms	4 Hz
1	1	1	1	500 ms	2 Hz	500 ms	2 Hz

- **Initialization of the Time and the Start Sequence**

The first update of the time occurs about 500ms later after the SET bit of control register B is reset. So keep followings in mind when initializing and adjusting the time.

Procedure of time initialization

(1) Set the SET bit of control register B. (SET = "1")
(2) Set "1" into all the DV0, 1, 2 bits of control register A. (DV0 = DV1 = DV2 = "1")
(3) Set the time and calendar to each RAM.
(4) Set the frequency in use into DV0, 1 and DV2.
(5) Reset the SET bit. (SET = "0")

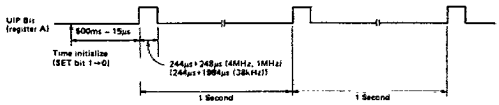


Figure 15 Time Initialization and the First Update

Restriction on Time-of-day and Calendar Initialization

There is a case in HD146818 (RTC) that update is not executed correctly if time of day and calendar shown below are initialized. Therefore, initialize the RTC without using time of day shown below.

Calendar, Time of day & Status after Update	Examples
If 29th 23:59:59 in all the months is initialized, update to 1st in the next month is executed. (Jan. – Dec. However except for Feb. 29th in leap year)	Mar. 29th →Apr. 1st
If 30th 23:59:59 in Apr., June, Sept., and Nov. is initialized, update to 31st in each month is executed.	Apr. 30th →Apr. 31st
If Feb. 28th 23:59:59 (not in leap year) is initialized, update to Feb. 29th is executed.	Feb. 28th, 1983 →Feb. 29th, 1983
If Feb. 28th 23:59:58 (in leap year) is initialized, update to Mar. 1st is executed.	Feb. 28th, 1984 →Mar. 1st, 1984

■ UPDATE CYCLE

The HD146818 executes an update cycle once-per-second, assuming one of the proper time bases is in place, the divider is not clear, and the SET bit in Register B is clear. The SET bit in the "1" state permits the program to initialize the time and calendar bytes by stopping an existing update and preventing a new one from occurring.

The primary function of the update cycle is to increment the seconds byte, check for overflow, increment the minutes byte when appropriate and so forth through to the year of the century byte. The update cycle also compares each alarm byte with the corresponding time byte and issues an alarm if a match or if a "don't care" code (11XXXXXX) is present in all three positions.

With a 4.194304 MHz or 1.048576 MHz time base the up-

date cycle takes 248 μs while a 32.768 kHz time base update cycle takes 1984 μs. During the update cycle, the time, calendar, and alarm bytes are not accessable by the processor program. The HD146818 protects the program from reading transitional data. This protection is provided by switching the time, calendar, and alarm portion of the RAM off the microprocessor bus during the entire update cycle. If the processor reads these RAM locations before the update is complete the output will be undefined. The update in progress (UIP) status bit is set during the interval.

A program which randomly accesses the time and date information finds data unavailable statistically once every 4032 attempts. Three methods of accommodating nonavailability during update are usable by the program. In discussing the three methods it is assumed that at random points user programs are able to call a subroutine to obtain the time of day.

The first method of avoiding the update cycle uses the update-ended interrupt. If enabled, an interrupt occurs after every update cycle which indicates that over 999 ms are available to read valid time and date information. During this time a display could be updated or the information could be transfered to continuously available RAM. Before leaving the interrupt service routine, the IRQF bit in Register C should be cleared.

The second method uses the update-in-progress bit (UIP) in Register A to determine if the update cycle is in progress or not. The UIP bit will pulse once-per-second. Statistically, the UIP bit will indicate that time and date information is unavailable once every 2032 attempts. After the UIP bit goes "1", the update cycle begins 244 μs later. Therefore, if a "0" is read on the UIP bit, the user has at least 244 μs before the time/calendar data will be changed. If a "1" is read in the UIP bit, the time/calendar data may not be valid. The user should avoid interrupt service routines that would cause the time needed to read valid time/calendar data to exceed 244 μs.

The third method uses a periodic interrupt to determine if an update cycle is in progress. The UIP bit in Register A is set "1" between the setting of the PF bit in Register C (see Figure 16) Periodic interrupts that occur at a rate of greater than $t_{BUC} + t_{UC}$ allow valid time and date information to be read at each occurrence of the periodic interrupt. The reads should be completed within $(t_{PI} \div 2) + t_{BUC}$ to insure that data is not read during the update cycle.

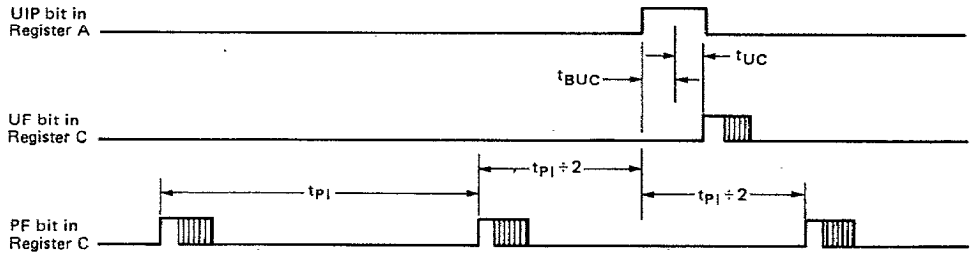
■ POWER-DOWN CONSIDERATIONS

In most systems, the HD146818 must continue to keep time when system power is removed. In such systems, a conversion from system power to an alternate power supply, usually a battery, must be made. During the transition from system to battery power, the designer of a battery backed-up RTC system must protect data integrity, minimize power consumption, and ensure hardware reliability according to the specification described in the section regarding Battery Backed-up operation.

The chip enable ($\overline{CE}$) pin controls all bus inputs (R/$\overline{W}$, $\overline{DS}$, AS, $AD_0 \sim AD_7$). $\overline{CE}$, when negated, disallows any unintended modification of the RTC data by the bus. $\overline{CE}$ also reduces power consumption by reducing the number of transitions seen internally.

Power consumption may be further reduced by removing resistive and capacitive loads from the clock out (CKOUT) pin and the squarewave (SQW) pin.

During and after the power source conversion, the V_{IN} maximum specification must never be exceeded. Failure to meet the V_{IN} maximum specification can cause a virtual SCR to appear which may result in excessive current drain and destruction of the part.



t_{PI} = Periodic Interrupt Time Interval (500 ms, 250 ms, 125 ms, 62.5 ms, etc.)
t_{UC} = Update Cycle Time (248 μs or 1984 μs)
t_{BUC} = Delay Time Before Update Cycle (244 μs)

Figure 16 Update-Ended and Periodic Interrupt Relationship

■ SIGNAL DESCRIPTIONS

The block diagram in Figure 10, shows the pin connection with the major internal functions of the HD146818 Real-Time Clock plus RAM. The following paragraphs describe the function of each pin.

• V_{CC}, V_{SS}

DC power is provided to the part on these two pins, V_{CC} being the most positive voltage. The minimum and maximum voltages are listed in the Electrical Characteristics tables.

• OSC_1, OSC_2 – Time Base (Inputs)

The time base for the time functions may be an external signal or the crystal oscillator. External square waves at 4.194304 MHz, 1.048576 MHz, or 32.768 kHz may be connected to OSC_1 as shown in Figure 17. The time-base frequency to be used is chosen in Register A.

The on-chip oscillator is designed for a parallel resonant crystal at 4.194304 MHz or 1.048576 MHz or 32.768 kHz frequencies. The crystal connections are shown in Figure 11.

• CKOUT – Clock Out (Output)

The CKOUT pin is an output at the time-base frequency divided by 1 or 4. A major use for CKOUT is as the input clock to the microprocessor; thereby saving the cost of a second crystal. The frequency of CKOUT depends upon the time-base frequency and the state of the CKFS pin as shown in Table 5.

• CKFS – Clock Out Frequency Select (Input)

The CKOUT pin is an output at the time-base frequency divided by 1 or 4. CKFS tied to V_{CC} causes CKOUT to be the same frequency as the time base at the OSC_1 pin. When CKFS is at V_{SS}, CKOUT is the OSC_1 time-base frequency divided by four. Table 5 summarizes the effect of CKFS.

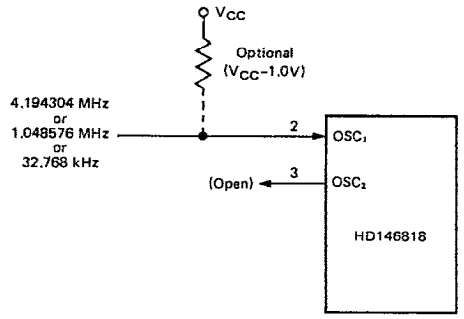


Figure 17 External Time-Base Connection

Table 5 Clock Output Frequencies

Time Base (OSC_1) Frequency	Clock Frequency Select Pin (CKFS)	Clock Frequency Output Pin (CKOUT)
4.194304 MHz	"High"	4.194304 MHz
4.194304 MHz	"Low"	1.048576 MHz
1.048576 MHz	"High"	1.048576 MHz
1.048576 MHz	"Low"	262.144 kHz
32.768 kHz	"High"	32.768 kHz
32.768 kHz	"Low"	8.192 kHz

• SQW – Square Wave (Output)

The SQW pin can output a signal one of 15 of the 22 internal-divider stages. The frequency and output enable of the SQW may be altered by programming Register A, as shown in Table 4. The SQW signal may be turned on and off using a bit in Register B.

• $AD_0 \sim AD_7$ – Multiplexed Bidirectional Address/Data Bus

Multiplexed bus processors save pins by presenting the address during the first portion of the bus cycle and using the same pins during the second portion for data. Address-then-data multiplexing does not slow the access time of the HD146818 since the bus reversal from address to data is occurring during the internal RAM access time.

The address must be valid just prior to the fall of AS/ALE at which time the HD146818 latches the address from AD_0 to AD_5. Valid write data must be presented and held stable during the latter portion of the DS or $\overline{WR}$ pulses. In a read cycle, the HD146818 outputs 8 bits of data during the latter portion of the DS or $\overline{RD}$ pulses, then ceases driving the bus (returns the output drivers to three-state) when DS falls in the HD6801, HD6301 case or $\overline{RD}$ rises in the other case.

• AS – Multiplexed Address Strobe (Input)

A positive going multiplexed address strobe pulse serves to demultiplex the bus. The falling edge of AS or ALE causes the address to be latched within the HD146818. The bus control circuit in the HD146818 also latches the state of the DS pin with the falling edge of AS or ALE.

• DS – Data Strobe or Read (Input)

The DS pin has two interpretations via the bus control circuit. When emanating from 6801 family type processor, DS is a positive pulse during the latter portion of the bus cycle, and is variously called DS (data strobe), E (enable), and ϕ_2 (ϕ_2 clock). During read cycles, DS signifies the time that the RTC is to drive the bidirectional bus. In write cycles, the trailing edge of DS causes the Real-Time Clock plus RAM to latch the written data.

The second interpretation of DS is that of $\overline{RD}$, $\overline{MEMR}$, or $\overline{I/OR}$ emanating from the 8085 type processor. In this case, DS identifies the time period when the real-time clock plus RAM drives the bus with read data. This interpretation of

DS is also the same as an output-enable signal on a typical memory.

The bus control circuit, within the HD146818, latches the state of the DS pin on the falling edge of AS/ALE. When 6801 mode, DS must be "Low" during AS/ALE, which is the case with 6801 family multiplexed bus processors. To insure the 8085 mode of this circuit the DS pin must remain "High" during the time AS/ALE is "High".

- **R/$\overline{W}$ – Read/Write (Input)**

The bus control circuit treats the R/$\overline{W}$ pin in one of two ways. When 6801 family type processor is connected, R/$\overline{W}$ is a level which indicates whether the current cycle is a read or write. A read cycle is indicated with a "High" level on R/$\overline{W}$ while DS is "High", whereas a write cycle is a "Low" on R/$\overline{W}$ during DS

The second interpretation of R/$\overline{W}$ is as a negative write pulse, $\overline{WR}$, $\overline{MEMW}$, and $\overline{I/OW}$ from 8085 type processors. This circuit in this mode gives R/$\overline{W}$ pin the same meaning as the write ($\overline{W}$) pulse on many generic RAMs.

- **$\overline{CE}$ – Chip Enable (Input)**

The chip-enable ($\overline{CE}$) signal must be asserted ("Low") for a bus cycle in which the HD146818 is to be accessed. $\overline{CE}$ is not latched and must be stable during DS and AS (in the 6801 case) and during $\overline{RD}$ and $\overline{WR}$ (in the 8085 case). Bus cycles which take place without asserting $\overline{CE}$ cause no actions to take place within the HD146818. When $\overline{CE}$ is "High", the multiplexed bus output is in a high-impedance state.

When $\overline{CE}$ is "High", all address, data, DS, and R/$\overline{W}$ inputs from the processor are disconnected within the HD146818. This permits the HD146818 to be isolated from a powered-down processor. When $\overline{CE}$ is held "High", an unpowered device cannot receive power through the input pins from the real-time clock power source. Battery power consumption can thus be reduced by using a pullup resistor or active clamp on $\overline{CE}$ when the main power is off.

- **$\overline{IRQ}$ – Interrupt Request (Output)**

The $\overline{IRQ}$ pin is an active "Low" output of the HD146818 that may be used as an interrupt input to a processor. The $\overline{IRQ}$ output remains "Low" as long as the status bit causing the interrupt is present and the corresponding interrupt-enable bit is set. To clear the $\overline{IRQ}$ pin, the processor program normally reads Register C. The $\overline{RES}$ pin also clears pending interrupts.

When no interrupt conditions are present, the $\overline{IRQ}$ level is in the high-impedance state. Multiple interrupting devices may thus be connected to an $\overline{IRQ}$ bus with one pullup at the processor.

- **$\overline{RES}$ – Reset (Input)**

The $\overline{RES}$ pin does not affect the clock, calendar, or RAM functions. On powerup, the $\overline{RES}$ pin must be held "Low" for the specified time, t_{RLH}, in order to allow the power supply to stabilize, Figure 18 shows a typical representation of the $\overline{RES}$ pin circuit.

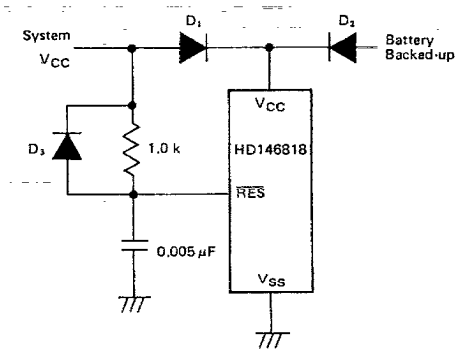
When $\overline{RES}$ is "Low" the following occurs:

a) Periodic Interrupt Enable (PIE) bit is cleared to "0".
b) Alarm Interrupt Enable (AIE) bit is cleared to "0".
c) Update ended interrupt Enable (UIE) bit is cleared to "0".
d) Update ended Interrupt Flag (UF) bit is cleared to "0".
e) Interrupt Request status Flag (IRQF) bit is cleared to "0".
f) Periodic Interrupt Flag (PF) bit is cleared to "0".
g) Alarm Interrupt Flag (AF) bit is cleared to "0".
h) $\overline{IRQ}$ pin is in high-impedance state, and
i) Square Wave output Enable (SQWE) bit is cleared to "0".

- **PS – Power Sense (Input)**

The power-sense pin is used in the control of the valid RAM and time (VRT) bit in Register C. When the PS pin is "Low" the VRT bit is cleared to "0".

During powerup, the PS pin must be externally held "Low" for the specified time, t_{PLH}. As power is applied the VRT bit remain "Low" indicating that the contents of the RAM, time registers, and calendar are not guaranteed. When normal operation commences PS should be permitted to go "High". Output signal from external power sence circuit will be connected to this input.



(NOTE) If the RTC is isolated from the MPU or MCU power by a diode drop, care must be taken to meet V_{in} requirements.

Figure 18 Typical Powerup Delay Circuit for $\overline{RES}$

■ REGISTERS

The HD146818 has four registers which are accessible to the processor program. The four registers are also fully accessible during the update cycle.

- **Register A ($0A)**

MSB							LSB	
b7	b6	b5	b4	b3	b2	b1	b0	Read/Write Register except UIP
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0	

UIP - The update in progress (UIP) bit is a status flag that may be monitored by the program. When UIP is a "1" the update

Table 6 Update Cycle Times

UIP Bit	Time Base (OSC_1)	Update Cycle Time (t_{UC})	Minimum Time Before Update Cycle (t_{BUC})
1	4.194304 MHz	248 μs	–
1	1.048576 MHz	248 μs	–
1	32.768 kHz	1984 μs	–
0	4.194304 MHz	–	244 μs
0	1.048576 MHz	–	244 μs
0	32.768 kHz	–	244 μs

cycle is in progress or will soon begin. When UIP is a "0" the update cycle is not in progress and will not be for at least 244 μs (for all time bases). This is detailed in Table 6. The time, calendar, and alarm information in RAM is fully available to the program when the UIP bit is zero – it is not in transition. The UIP bit is a read-only bit, and is not affected by Reset. Writing the SET bit in Register B to a "1" inhibit any update cycle and then clear the UIP status bit.

DV2, DV1, DV0 – Three bits are used to permit the program to select various conditions of the 22-stage divider chain. The divider selection bits identify which of the three time-base frequencies is in use. Table 3 shows that time bases of 4.194304 MHz, 1.048576 MHz, and 32.768 kHz may be used. The divider selection bits are also used to reset the divider chain. When the time/calendar is first initialized, the program may start the divider at the precise time stored in the RAM. When the divider reset is removed the first update cycle begins half a second later. These three read/write bits are never modified by the RTC and are not affected by $\overline{RES}$.

RS3, RS2, RS1, RS0 – The four rate selection bits select one of 15 taps on the 22-stage divider, or disable the divider output. The tap selected may be used to generate an output square wave (SQW pin) and/or a periodic interrupt. The program may do one of the following: 1) enable the interrupt with the PIE bit, 2) enable the SQW output pin with the SQWE bit, 3) enable both at the same time at the same rate, or 4) enable neither. Table 4 lists the periodic interrupt rates and the square-wave frequencies that may be chosen with the RS bits. These four bits are read/write bits which are not affected by $\overline{RES}$ and are never changed by the RTC.

- **Register B ($0B)**

MSB LSB — Read/Write Register

b7	b6	b5	b4	b3	b2	b1	b0
SET	PIE	AIE	UIE	SQWE	DM	24/12	DSE

SET When the SET bit is a "0", the update cycle functions normally by advancing the counts once-per-second. When the SET bit is written to a "1", any update cycle in progress is aborted and the program may initialize the time and calendar bytes without an update occurring in the midst of initializing. SET is a read/write bit which is not modified by $\overline{RES}$ or internal functions of the HD146818.

PIE – The periodic interrupt enable (PIE) bit is a read/write bit which allows the periodic-interrupt flag (PF) bit to cause the $\overline{IRQ}$ pin to be driven "Low". A program writes a "1" to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3, RS2, RS1, and RS0 bits in Control Register A. A "0" in PIE blocks $\overline{IRQ}$ from being initiated by a periodic interrupt, but the periodic flag (PF) bit is still at the periodic rate. PIE is not modified by any internal HD146818 functions, but is cleared to "0" by a $\overline{RES}$.

AIE – The alarm interrupt enable (AIE) bit is a read/write bit which when set to a "1" permits the alarm flag (AF) to assert $\overline{IRQ}$. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including a "don't care" alarm code of binary 11XXXXXX). When the AIE bit is a "0", the AF bit does not initiate an $\overline{IRQ}$ signal. The $\overline{RES}$ pin clears AIE to "0". The internal functions do not affect the AIE bit.

UIE – The UIE (update-ended interrupt enable) bit is a read/write bit which enables the update-end flage (UF) bit to assert $\overline{IRQ}$. The $\overline{RES}$ pin going "Low" or the SET bit going "1" clears the UIE bit.

SQWE – When the square-wave enable (SQWE) bit is set to a "1" by the program, a square-wave signal at the frequency specified in the rate selection bits (RS3 to RS0) appears on the SQW pin. When the SQWE bit is set to a "0" the SQW pin is held "Low". The state of SQWE is cleared by the $\overline{RES}$ pin. SQWE is a read/write bit.

DM – The data mode (DM) bit indicates whether time and calendar updates are to use binary or BCD formats. The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or $\overline{RES}$. A "1" in DM signifies binary data, while a "0" in DM specified binary-coded-decimal (BCD) data.

24/12 – The 24/12 control bit establishes the format of the hours bytes as either the 24-hour mode (a "1") or the 12-hour mode (a "0"). This is a read/write bit, which is affected only by the software.

DSE – The daylight savings enable (DSE) bit is a read/write bit which allows the program to enable two special updates (when DSE is a "1"). On the last Sunday in April the time increments from 1:59:59 AM to 3:00:00 AM. On the last Sunday in October when the time first reaches 1:59:59 AM it changes to 1:00:00 AM. These special updates do not occur when the DSE bit is a "0". DSE is not changed by any internal operations or reset.

- **Register C ($0C)**

MSB LSB — Read-Only Register

b7	b6	b5	b4	b3	b2	b1	b0
IRQF	PF	AF	UF	0	0	0	0

IRQF – The interrupt request flag (IRQF) is set to a "1" when one or more of the following are true:

PF = PIE = "1"
AF = AIE = "1"
UF = UIE = "1"

i.e., IRQF = PF · PIE + AF · AIE + UF · UIE

Any time the IRQF bit is a "1", the $\overline{IRQ}$ pin is driven "Low". All flag bits are cleared after Register C is read by the program or when the $\overline{RES}$ pin is low. A program write to Register C does not modify any of the flag bits.

PF – The periodic interrupt flag (PF) is a read-only bit which is set to a "1" when a particular edge is detected on the selected tap of the divider chain. The RS3 to RS0 bits establish the periodic rate. PF is set to a "1" independent of the state of the PIE bit. PF being a "1" initiates an $\overline{IRQ}$ signal and the IRQF bit when PIE is also a "1". The PF bit is cleared by a $\overline{RES}$ or a software read of Register C.

AF – A "1" in the AF (alarm interrupt flag) bit indicates that the current time has matched the alarm time. A "1" in the AF causes the $\overline{IRQ}$ pin to go "Low", and a "1" to appear in the IRQF bit, when the AIE bit also is a "1". A $\overline{RES}$ or a read

of Register C clears AF.

UF – The update-ended interrupt flag (UF) bit is set after each update cycle. When the UIE bit is a "1", the "1" in UF causes the IRQF bit to be a "1", asserting $\overline{IRQ}$. UF is cleared by a Register C read or a $\overline{RES}$.

b3 to b0 – The unused bits of Status Register C are read as "0's". They can not be written.

- **Register D ($0D)**

MSB LSB

b7	b6	b5	b4	b3	b2	b1	b0
VRT	0	0	0	0	0	0	0

Read Only Register

VRT – The valid RAM and time (VRT) bit indicates the condition of the contents of the RAM, provided the power sense (PS) pin is satisfactorily connected. A "0" appears in the VRT bit when the power-sense pin is "Low". The processor program can set the VRT bit when the time and calendar are initialized to indicate that the RAM and time are valid. The VRT is a read/only bit which is not modified by the $\overline{RES}$ pin. The VRT bit can only be set by reading the Register D. For setting this bit, PS signal needs to be "High" level.

b6 to b0 – The remaining bits of Register D are unused. They cannot be written, but are always read as "0's".

■ NOTE FOR USE

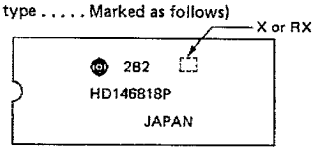
Input Signal, which is not necessary for user's application, should be used fixed to "High" or "Low" level. This is applicable to the following signal pins.

CKFS, PS

RESTRICTION ON HD146818 USAGE (1)

The daylight saving function can not be performed on the HD146818P (X type). So do not use this function for the system design.

< Type number > HD146818P (X type . . . . . Marked as follows)



< Restriction on usage >

Please set "0" to DSE bit (Daylight Saving Enable bit) on initializing the control register B.
DSE = "1" is prohibited.

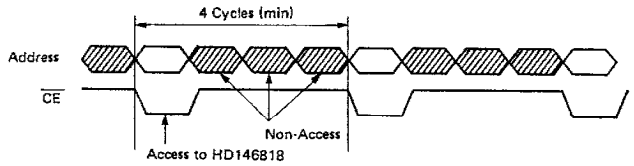
RESTRICTION ON HD146818 USAGE (2)

Access to HD146818 needs to be performed under following conditions.

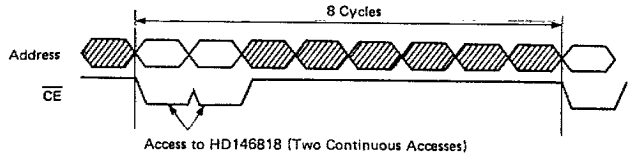
(i) Chip-enable ($\overline{CE}$) must be asserted to active "Low" level only when MPU performs read/write operation from/into internal RAM (Time and Calendar RAM, Control register, User RAM).

(ii) User RAM and control register must be accessed in less than 1/4 frequency shown below.
(Example: After one access, non-access cycles more than three cycles are necessary to be inserted.)

[Example 1]



[Example 2]



As shown in the above (example 2), when HD146818 is accessed continuously, continuous access must not be executed over fifty times.

(iii) The application that User RAM is used for program area should be avoided. (Inhibit continuous access.)

(iv) Minimize the noise by inserting noise bypass condenser between power supply and ground pin (V_{CC}-V_{SS}). (Insert noise bypass condenser as near HD146818 as possible.)

RESTRICTION ON HD146818 USAGE (3)

Chip-enable ($\overline{CE}$) must be stable between falling edge of DS and vising edge of AS shown below. (Address decoder hazard needs to be externally suppressed in this period.)